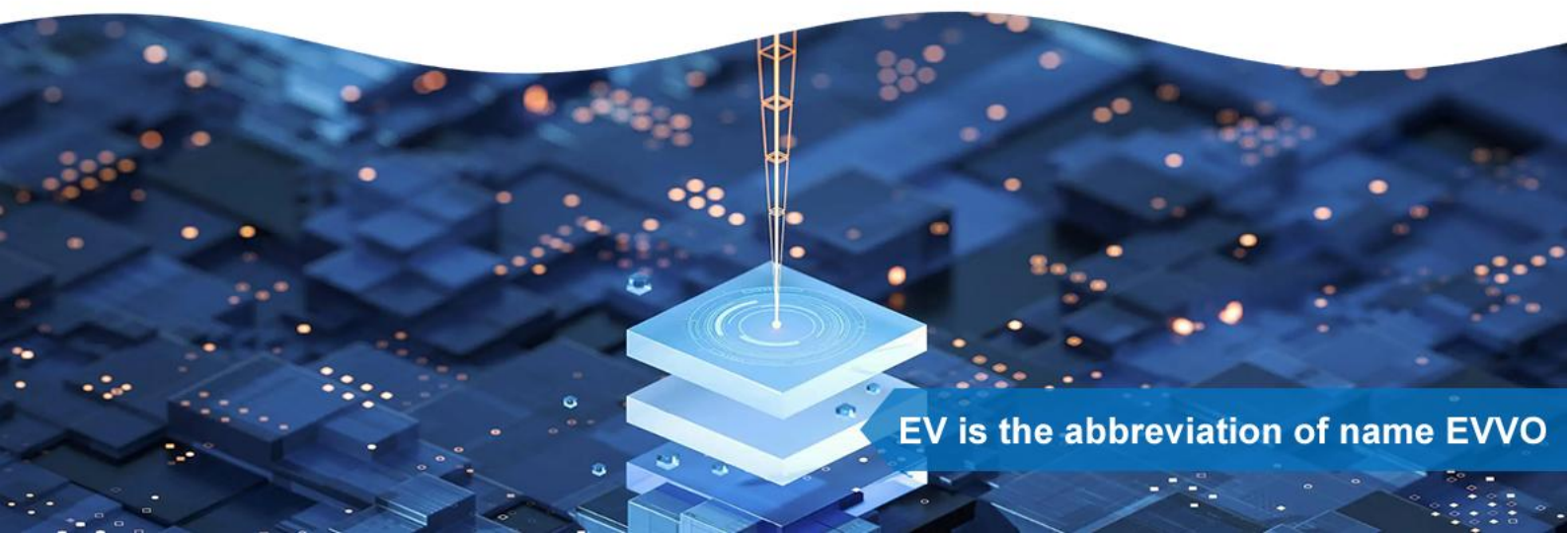
EVVOSEMI®
THINK CHANGE DO

ESD TVS MOS LDO Diode Sensor DC-DC

Product Specification

Domestic Part Number	IRF7309
Overseas Part Number	IRF7309
Equivalent Part Number	IRF7309



Dual N + P Channel MOSFET

Features

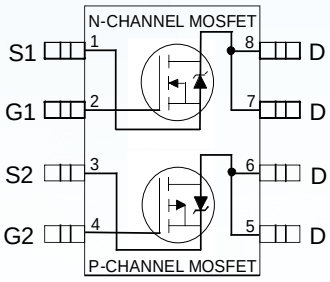
N-Ch:

- $V_{DS\ (V)}$ = 30V
- $R_{DS(ON)}$ < 50mΩ (V_{GS} = 4.5V)
- $R_{DS(ON)}$ < 70mΩ (V_{GS} = 2.7V)

P-Ch:

- $V_{DS\ (V)}$ = -30V
- $R_{DS(ON)}$ < 100mΩ (V_{GS} = 4.5V)
- $R_{DS(ON)}$ < 140mΩ (V_{GS} = 2.7V)

- Industry-standard pinout SO-8 Package
- Compatible with Existing Surface Mount Techniques



Top View

Benefits

- Multi-Vendor Compatibility
- Easier Manufacturing
- Environmentally Friendlier
- Increased Reliability

Absolute Maximum Ratings

Parameter		Max.		Units
		N-Channel	P-Channel	
I_D @ T_A = 25°C	10 Sec. Pulse Drain Current, V_{GS} @ 10V	4.7	-3.5	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	4.0	-3.0	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	3.2	-2.4	A
I_{DM}	Pulsed Drain Current ①	16	-12	A
P_D @T_A = 25°C	Power Dissipation (PCB Mount)**	1.4		W
	Linear Derating Factor (PCB Mount)**	0.011		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	6.9	-6.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Amb. (PCB Mount, steady state)**			90	°C/W

Dual N + P Channel MOSFET

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30			V	V_{GS} = 0V, I_D = 250μA
		P-Ch	-30				V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch		0.032		V/°C	Reference to 25°C, I_D = 1mA
		P-Ch		0.037			Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch			50	mΩ	V_{GS} = 10V, I_D = 2.4A ③
					70		V_{GS} = 4.5V, I_D = 2.0A ③
		P-Ch			100		V_{GS} = -10V, I_D = -1.8A ③
					140		V_{GS} = -4.5V, I_D = -1.5A ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0			V	V_{DS} = V_{GS}, I_D = 250μA
		P-Ch	-1.0				V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	N-Ch	5.2			S	V_{DS} = 15V, I_D = 2.4A ③
		P-Ch	2.5				V_{DS} = -24V, I_D = -1.8A ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch			1.0	μA	V_{DS} = 24V, V_{GS} = 0V
		P-Ch			-1.0		V_{DS} = -24V, V_{GS} = 0V
		N-Ch			25		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
		P-Ch			-25		V_{DS} = -24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	N-P			±100		V_{GS} = ± 20V
Q_g	Total Gate Charge	N-Ch			25	nC	N-Channel I_D = 2.6A, V_{DS} = 16V, V_{GS} = 4.5V ③ P-Channel I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V
		P-Ch			25		
Q_{gs}	Gate-to-Source Charge	N-Ch			2.9		
		P-Ch			2.9		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch			7.9		
		P-Ch			9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch		6.8		ns	N-Channel V_{DD} = 10V, I_D = 2.6A, R_G = 6.0Ω, R_D = 3.8Ω ③ P-Channel V_{DD} = -10V, I_D = -2.2A, R_G = 6.0Ω, R_D = 4.5Ω
		P-Ch		11			
t_r	Rise Time	N-Ch		21			
		P-Ch		17			
$t_{d(off)}$	Turn-Off Delay Time	N-Ch		22			
		P-Ch		25			
t_f	Fall Time	N-Ch		7.7			
		P-Ch		18			
L_D	Internal Drain Inductace	N-P		4.0		nH	Between lead tip and center of die contact
L_S	Internal Source Inductance	N-P		6.0			
C_{iss}	Input Capacitance	N-Ch		520		pF	N-Channel V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz ③ P-Channel V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz
		P-Ch		440			
C_{oss}	Output Capacitance	N-Ch		180			
		P-Ch		200			
C_{rss}	Reverse Transfer Capacitance	N-Ch		72			
		P-Ch		93			

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch			1.8	A	
		P-Ch			-1.8		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch			16		
		P-Ch			-12		
V_{SD}	Diode Forward Voltage	N-Ch			1.0	V	T_J = 25°C, I_S = 1.8A, V_{GS} = 0V ③
		P-Ch			-1.0		T_J = 25°C, I_S = -1.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	N-Ch		47	71	ns	N-Channel T_J = 25°C, I_F = 2.6A, di/dt = 100A/μs P-Channel T_J = 25°C, I_F = -2.2A, di/dt = 100A/μs ③
		P-Ch		53	80		
Q_{rr}	Reverse Recovery Charge	N-Ch		56	84	nC	
		P-Ch		66	99		
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)
② N-Channel I_{SD} ≤ 2.4A, di/dt ≤ 73A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C
P-Channel I_{SD} ≤ -1.8A, di/dt ≤ 90A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C
③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

N-Channel

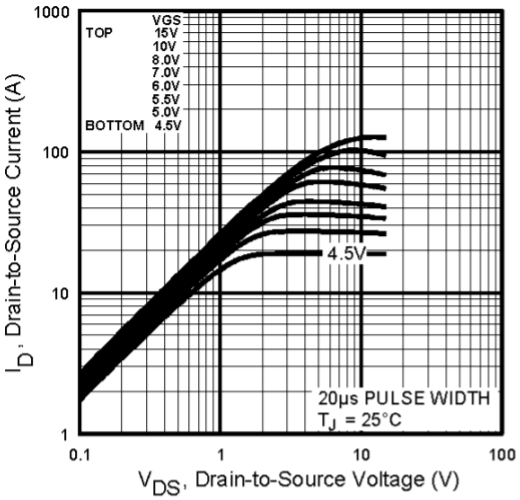


Fig 1. Typical Output Characteristics, T_J = 25ºC

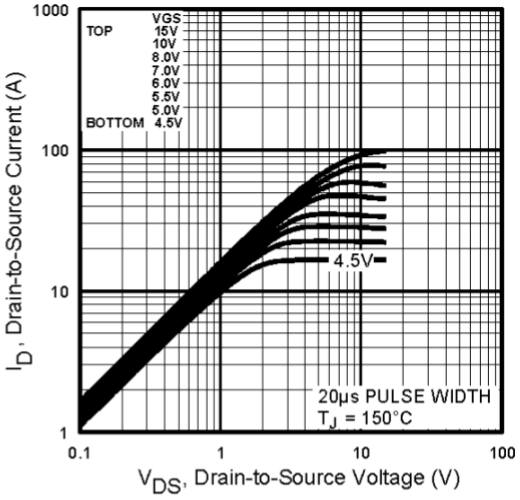


Fig 2. Typical Output Characteristics, T_J = 150ºC

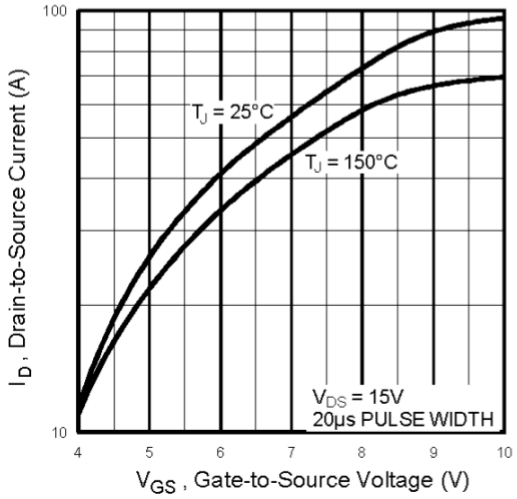


Fig 3. Typical Transfer Characteristics

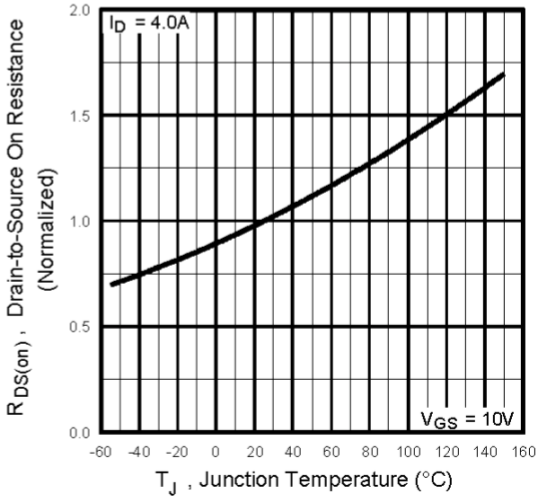


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel

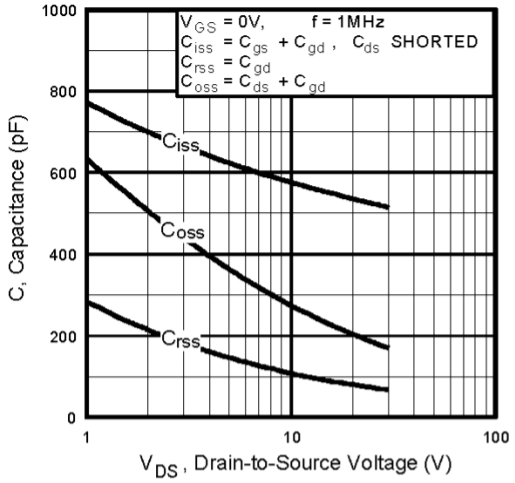


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

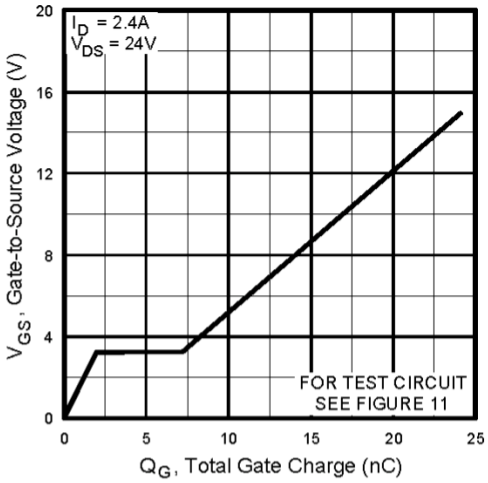


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

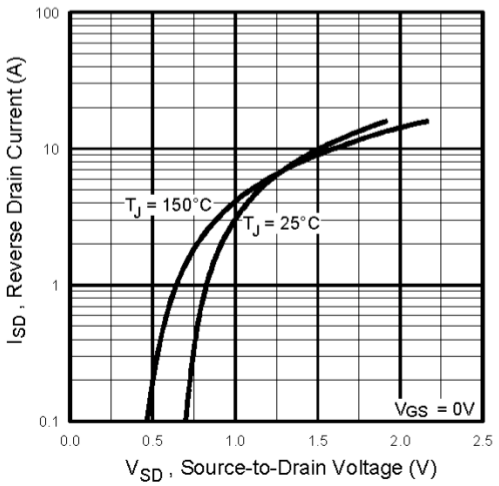


Fig 7. Typical Source-Drain Diode Forward Voltage

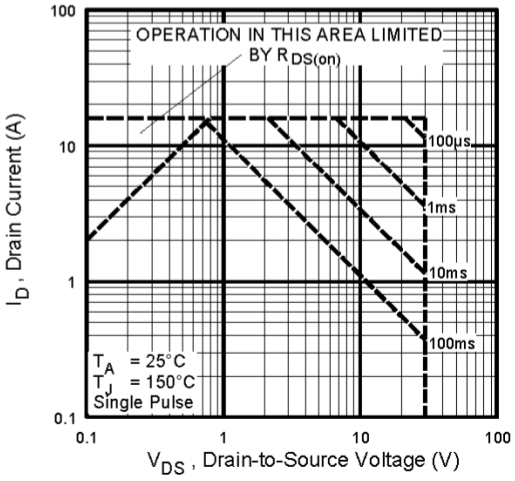


Fig 8. Maximum Safe Operating Area

N-Channel

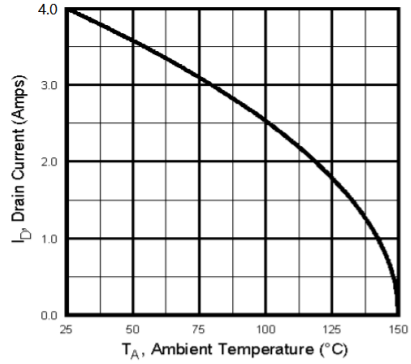


Fig 9. Max. Drain Current Vs. Ambient Temp.

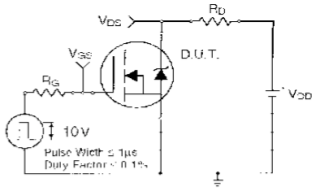


Fig 10a. Switching Time Test Circuit

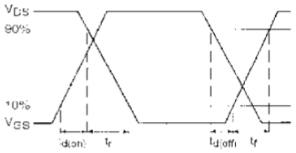


Fig 10b. Switching Time Waveforms

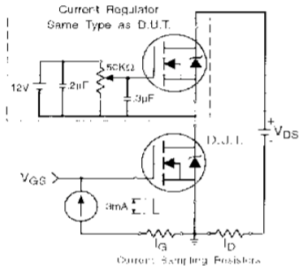


Fig 11a. Gate Charge Test Circuit

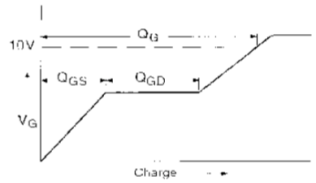


Fig 11b. Basic Gate Charge Waveform

P-Channel

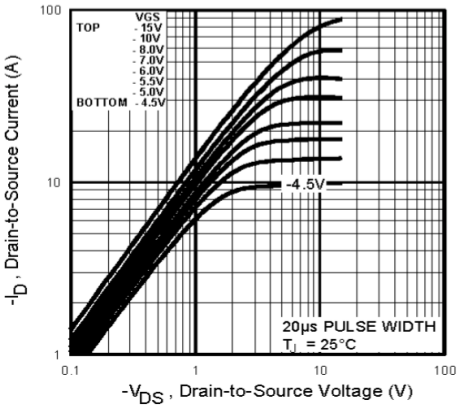


Fig 12. Typical Output Characteristics, T_J = 25ºC

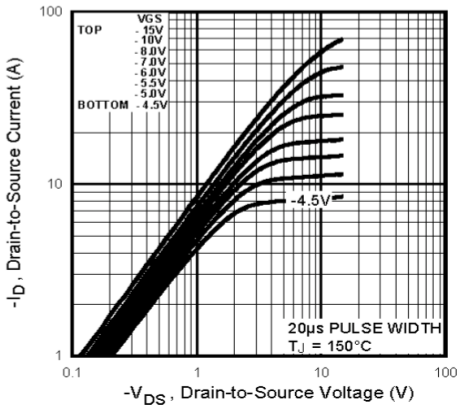


Fig 13. Typical Output Characteristics, T_J = 150ºC

P-Channel

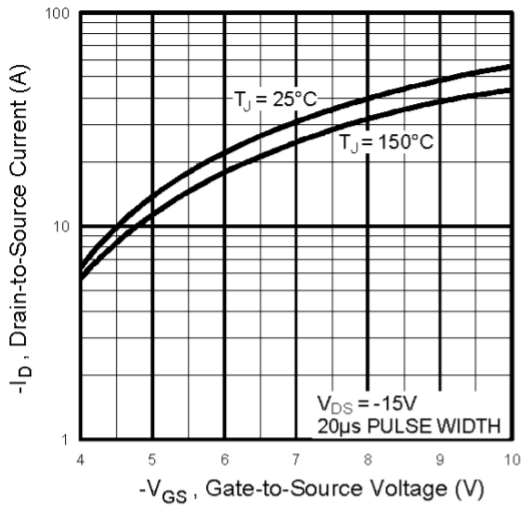


Fig 14. Typical Transfer Characteristics

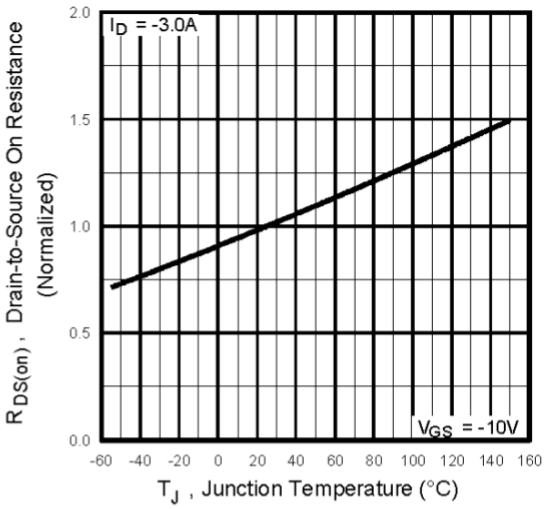


Fig 15. Normalized On-Resistance Vs. Temperature

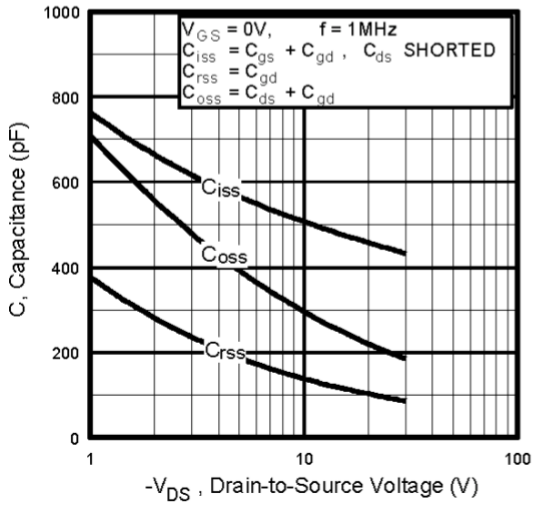


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

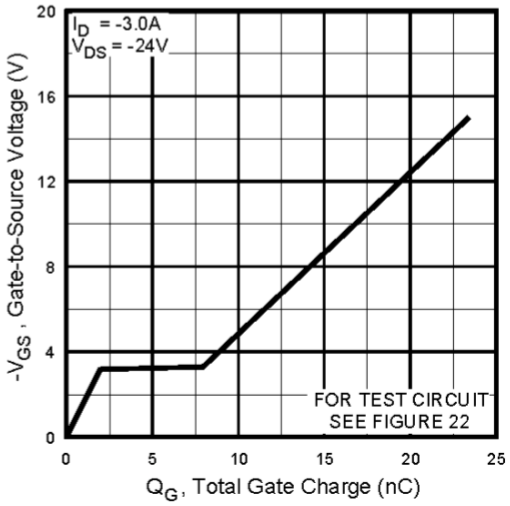


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

P-Channel

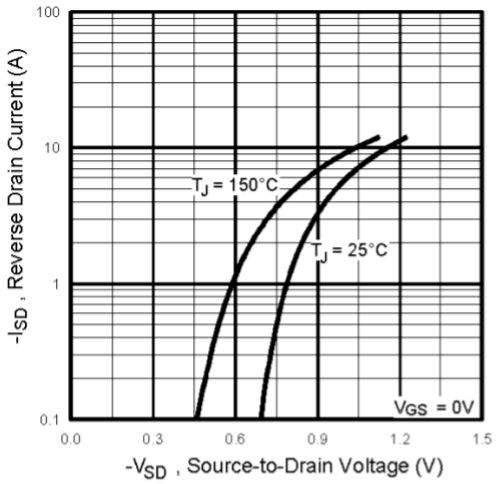


Fig 18. Typical Source-Drain Diode Forward Voltage

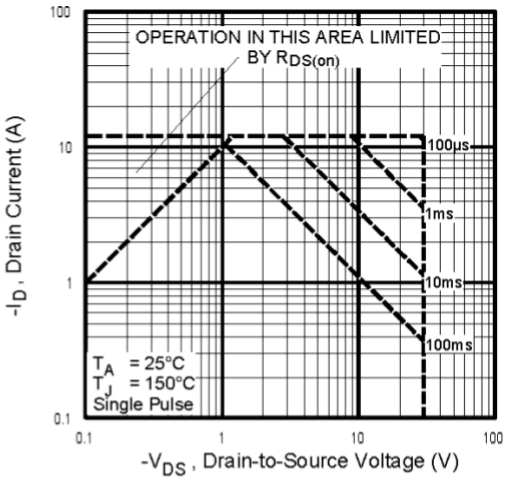


Fig 19. Maximum Safe Operating Area

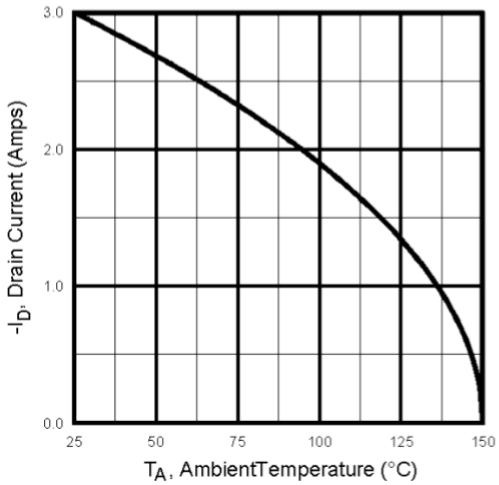


Fig 20. Max.Drain Current Vs. Ambient Temp.

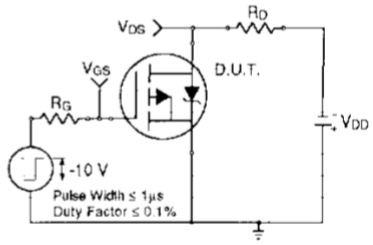


Fig 21a. Switching Time Test Circuit

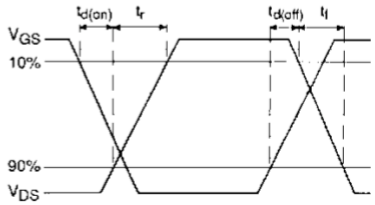


Fig 21b. Switching Time Waveforms

P-Channel

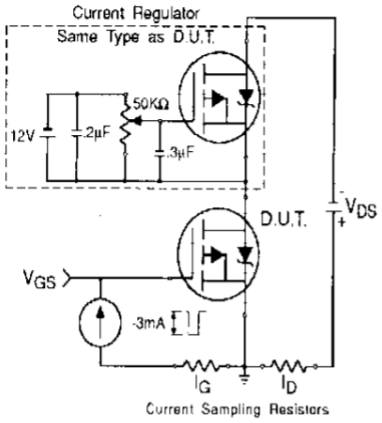


Fig 22b. Gate Charge Test Circuit

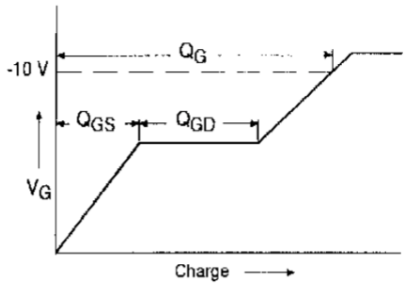


Fig 22b. Basic Gate Charge Waveform

N- and P-Channel

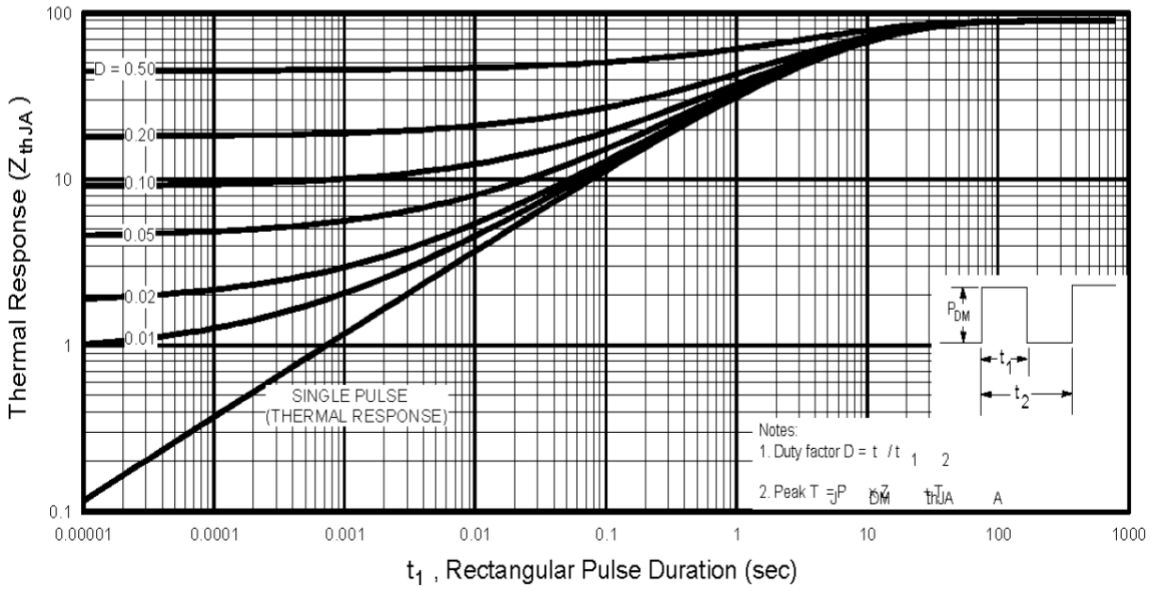
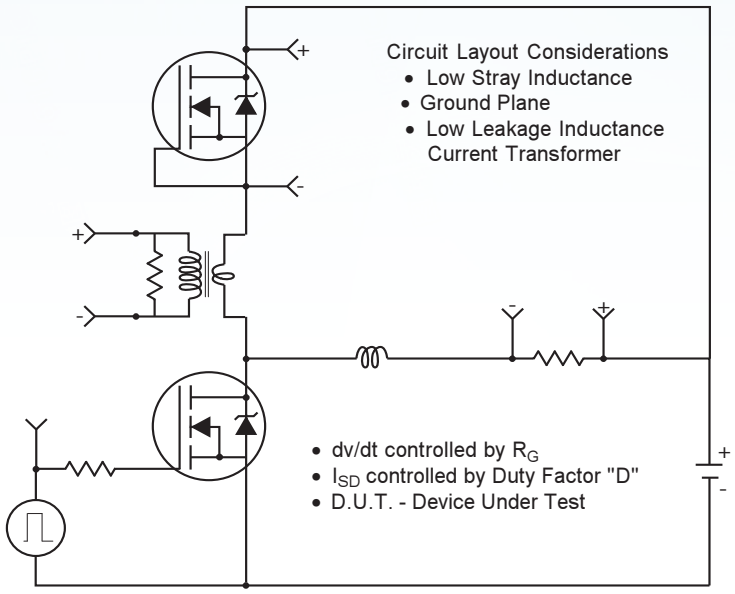


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

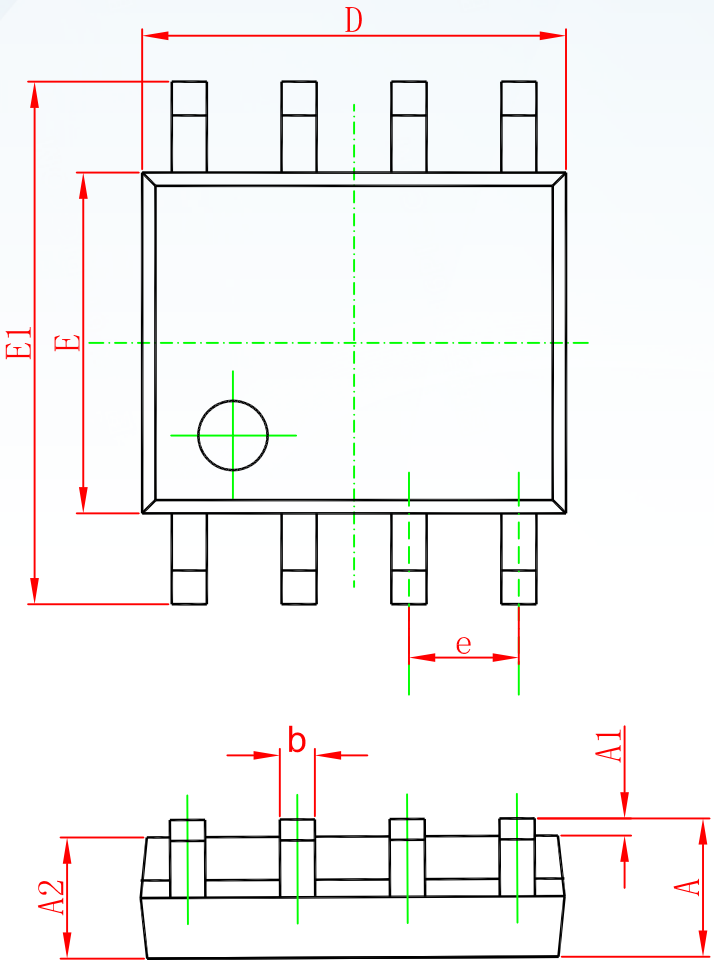
Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements

Dual N + P Channel MOSFET

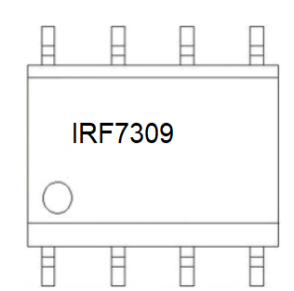
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Dual N + P Channel MOSFET

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
IRF7309	SOP-8	3000	Tape and reel

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