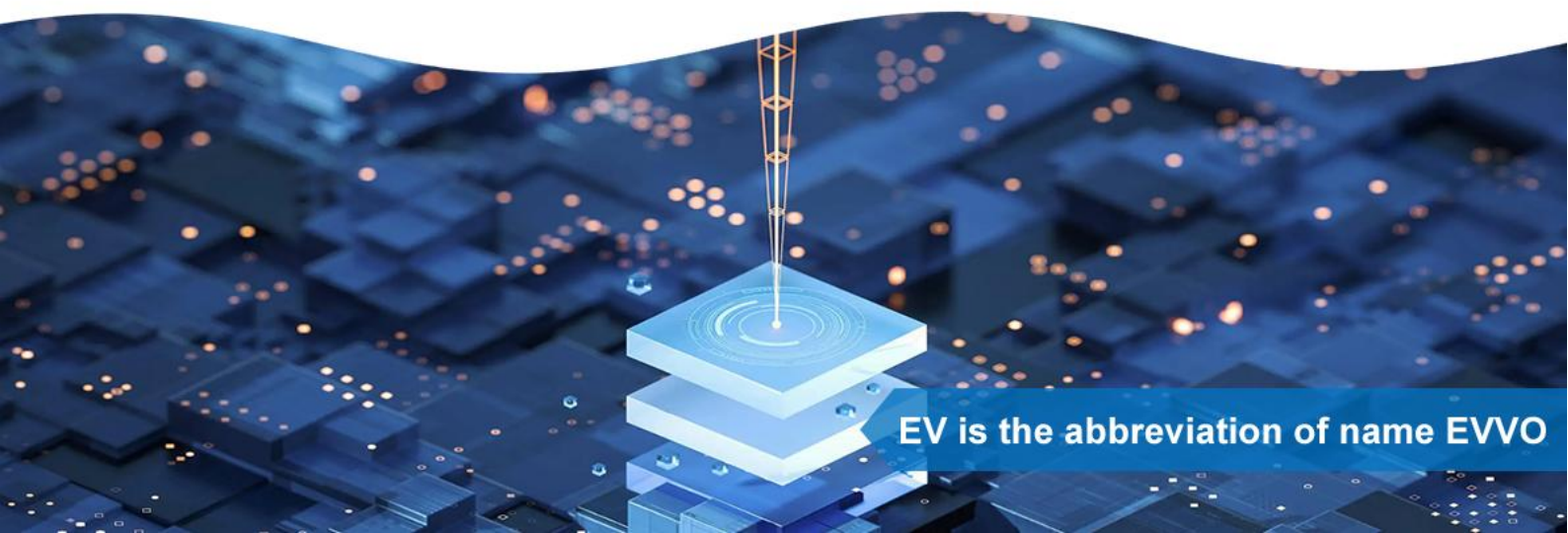
EVVOSEMI®
THINK CHANGE DO

ESD TVS MOS LDO Diode Sensor DC-DC

Product Specification

Domestic Part Number	IRF7507
Overseas Part Number	IRF7507
Equivalent Part Number	IRF7507



20V N+P-Channel Enhancement Mode MOSFET

Description

The IRF7507 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

GeneraFeatures

NMOS

V_{DS} = 20V I_D =2.3A

$R_{DS(ON)}$ < 55mΩ @ V_{GS}=10V

$R_{DS(ON)}$ < 70mΩ @ V_{GS}=4.5V

PMOS

V_{DS} = -20V I_D =-2.3 A

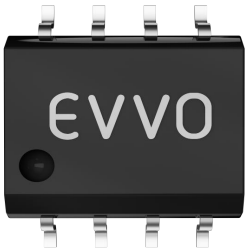
$R_{DS(ON)}$ < -110 mΩ @ V_{GS}=10V

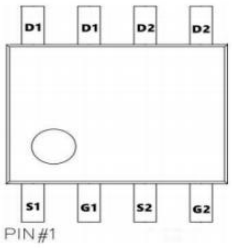
$R_{DS(ON)}$ < -140mΩ @ V_{GS}=4.5V

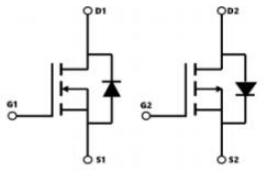
Applications

- Load/ Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

SOP8 Pin Configuration







Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
VDS	Drain-Source Voltage	20	-20	V
VGS	Gate-Source Voltage	±12	±12	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	5.8	-3.5	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	4.9	-2.8	A
IDM	Pulsed Drain Current[2]	20	-15	A
P_D@T_C=25℃	Total Power Dissipation[4]	1	1	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃
RθJA	Thermal Resistance Junction-Ambient [1]	125	125	℃/W
RθJC	Thermal Resistance Junction-Case[1]	85	95	℃/W

20V N+P-Channel Enhancement Mode MOSFET

N-Channel Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25°C , I_D=1mA	---	0.029	---	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=5.8A	---	---	27	mΩ
		V_{GS}=4.5V , I_D=5A	---	---	32	
		V_{GS}=2.5V , I_D=4A	---	---	40	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.5	---	1.2	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-2.82	---	mV/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V , T_J=25°C	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55°C	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=5A	---	25	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.5	---	
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=5.8A	---	11.5	---	nC
Q_{gs}	Gate-Source Charge		---	1.6	---	
Q_{gd}	Gate-Drain Charge		---	2.9	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3 I_D=5A	---	5	---	ns
T_r	Rise Time		---	47.	---	
$T_{d(off)}$	Turn-Off Delay Time		---	26	---	
T_f	Fall Time		---	8	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	860	---	pF
C_{oss}	Output Capacitance		---	84	---	
C_{rss}	Reverse Transfer Capacitance		---	70	---	

Note :

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The power dissipation is limited by 150°C junction temperature

4 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

20V N+P-Channel Enhancement Mode MOSFET

P-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	---	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.01	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-3A	---	60	75	mΩ
		V_{GS}=-2.5V , I_D=-2A	---	85	105	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.5	-0.7	-1.2	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.98	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-16V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-16V , V_{GS}=0V , T_J=55℃	---	---	-5	
IGSS	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-3A	---	9	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-5V , V_{GS}=-4.5V , I_D=-3A	---	9.7	13.6	nC
Qgs	Gate-Source Charge		---	2.05	2.9	
Qgd	Gate-Drain Charge		---	2.43	3.4	
Td(on)	Turn-On Delay Time	V_{DD}=-10V , V_{GS}=-4.5V , R_G=3.3 I_D=-3A	---	4.8	9.6	ns
T_r	Rise Time		---	9.6	17.3	
Td(off)	Turn-Off Delay Time		---	52	104	
T_f	Fall Time		---	8.4	16.8	
Ciss	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	686	960	pF
Coss	Output Capacitance		---	90.8	127	
Crss	Reverse Transfer Capacitance		---	80.4	113	
IS	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-3.1	A
ISM	Pulsed Source Current[2,4]		---	---	-15.5	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V
trr	Reverse Recovery Time	IF=-3A , dI/dt=100A/μs , T_J=25℃	---	8.4	---	nS
Q_{rr}	Reverse Recovery Charge		---	3.3	---	nC

Note :

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The power dissipation is limited by 150℃ junction temperature
4. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

20V N+P-Channel Enhancement Mode MOSFET

N-Channel Typical Characteristics

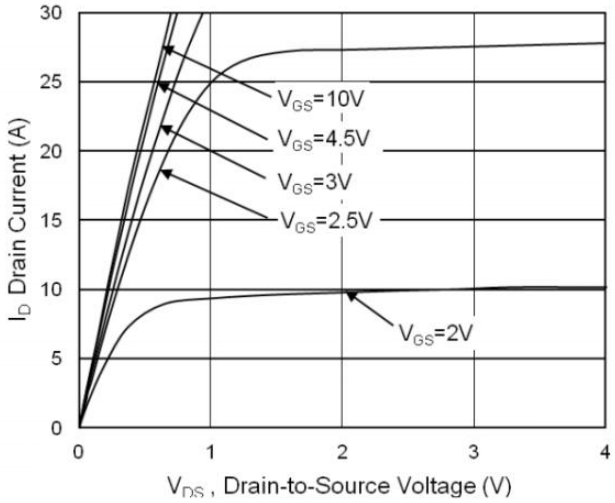


Fig.1 Typical Output Characteristics

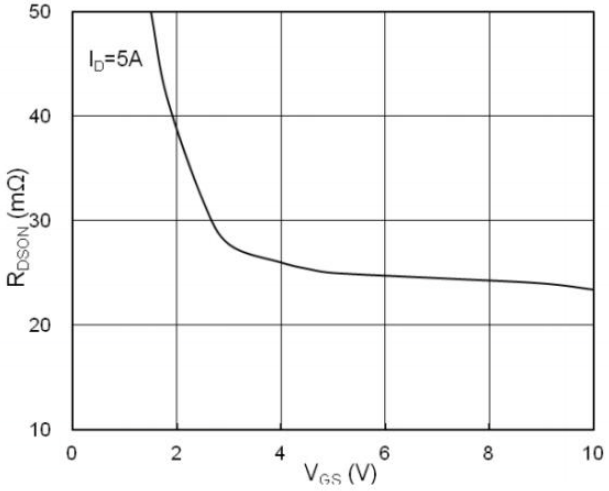


Fig.2 On-Resistance vs. Gate-Source

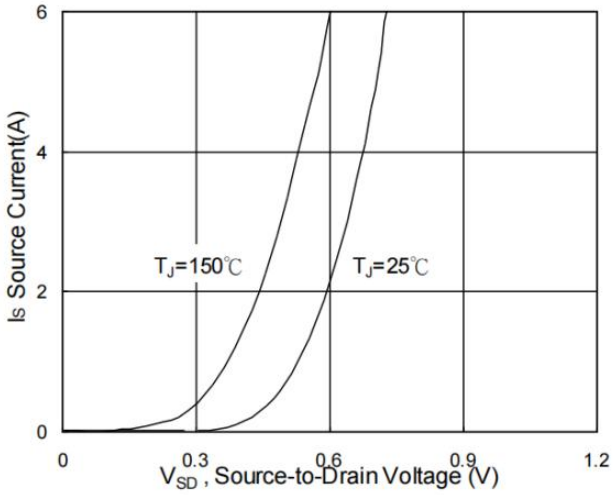


Fig.3 Forward Characteristics Of Reverse

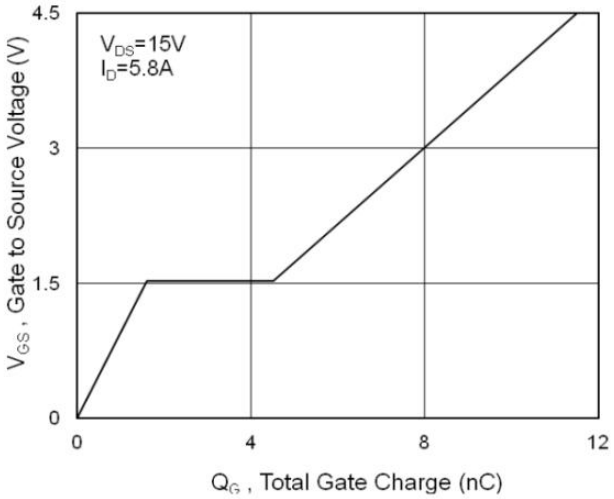


Fig.4 Gate-Charge Characteristics

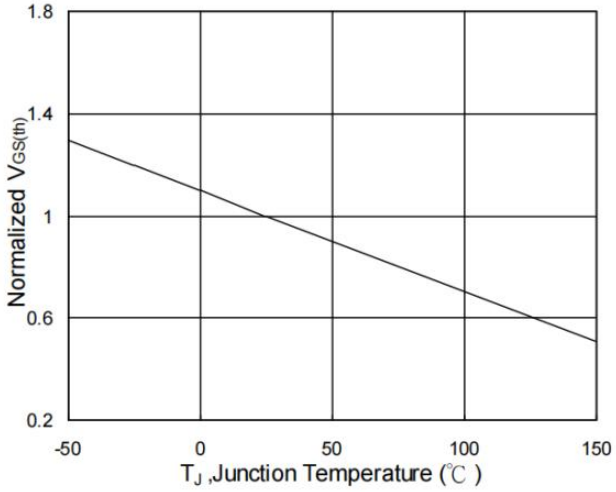


Fig.5 Normalized $V_{GS(th)}$ vs T_J

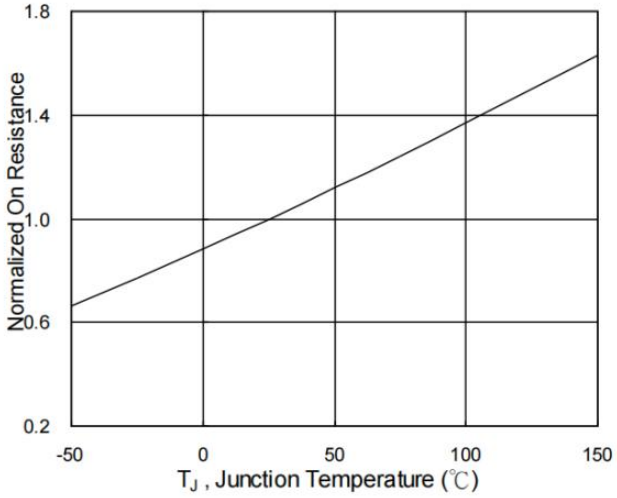


Fig.6 Normalized R_{DSON} vs T_J

20V N+P-Channel Enhancement Mode MOSFET

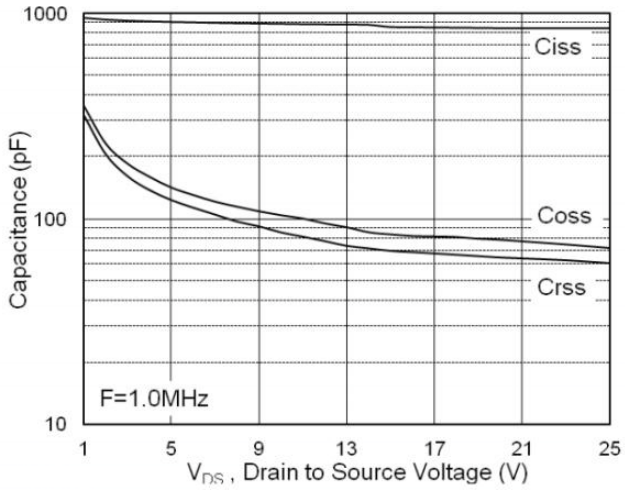


Fig.7 Capacitance

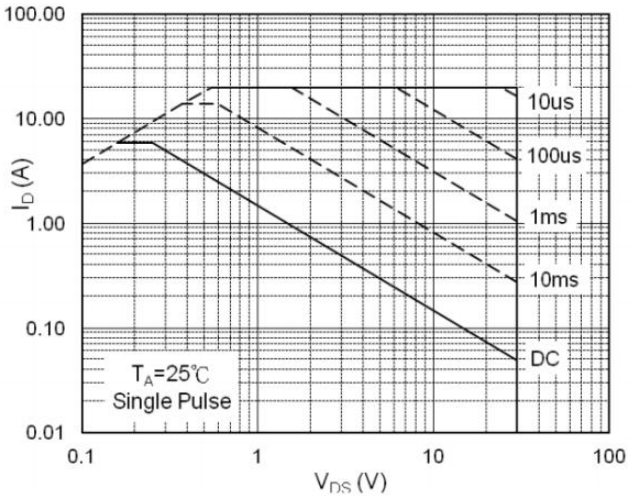


Fig.8 Safe Operating Area

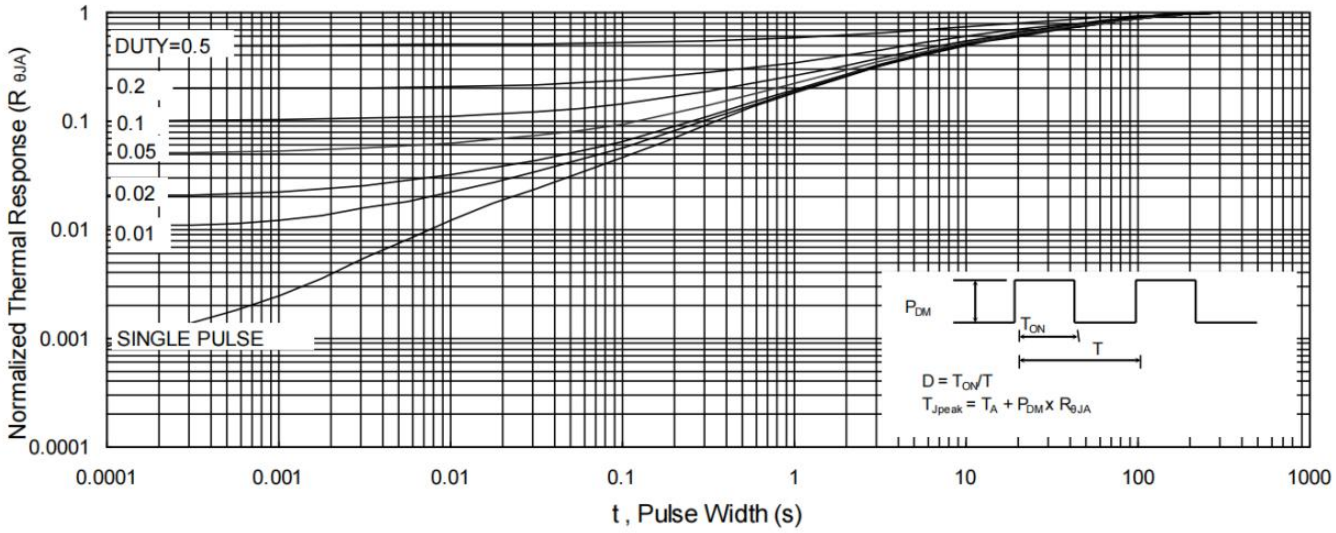


Fig.9 Normalized Maximum Transient Thermal Impedance

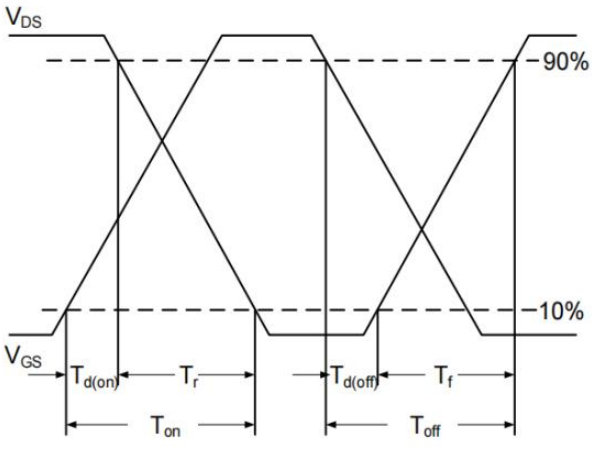


Fig.10 Switching Time Waveform

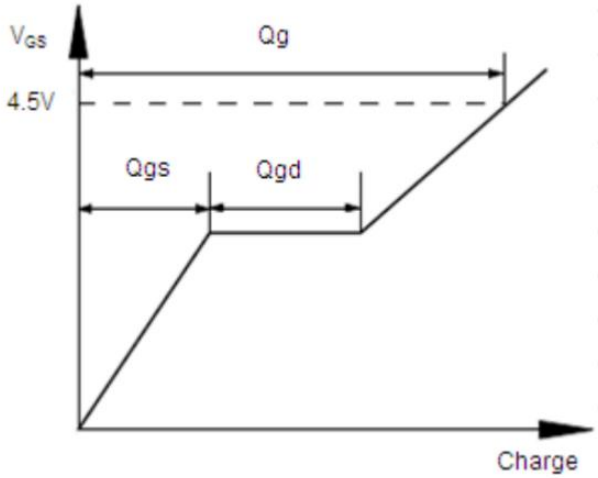


Fig.11 Gate Charge Waveform

P-Channel Typical Characteristics

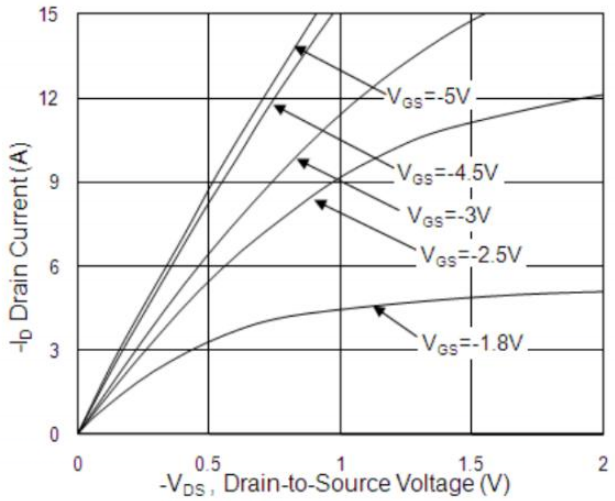


Fig.1 Typical Output Characteristics

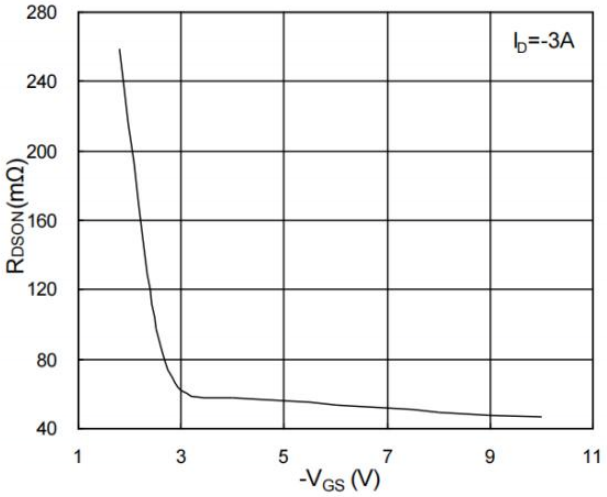


Fig.2 On-Resistance vs. Gate-Source

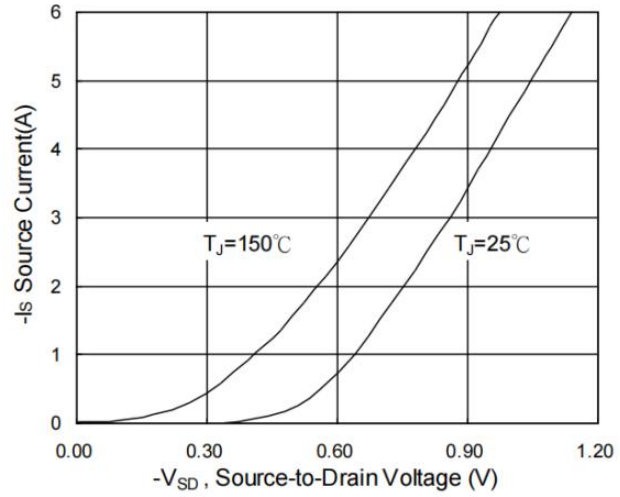


Fig.3 Forward Characteristics Of Reverse

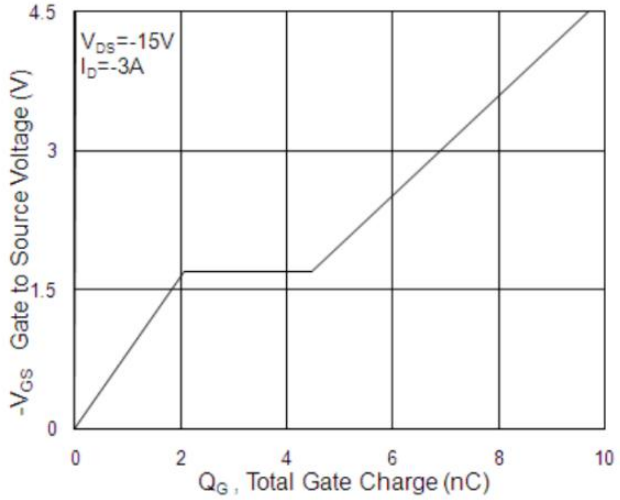


Fig.4 Gate-Charge Characteristics

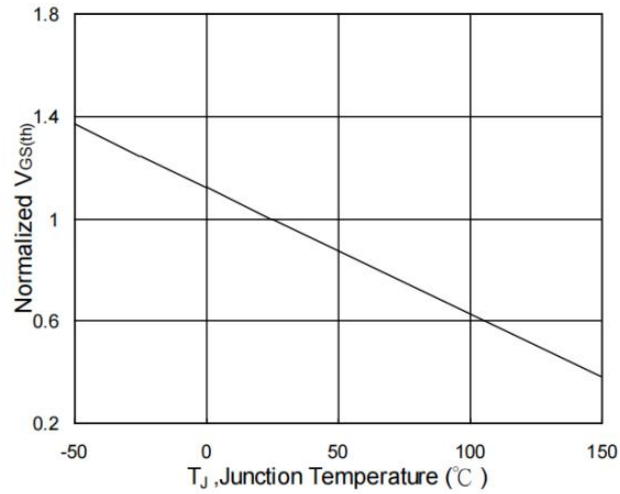


Fig.5 Normalized $V_{GS(th)}$ vs T_J

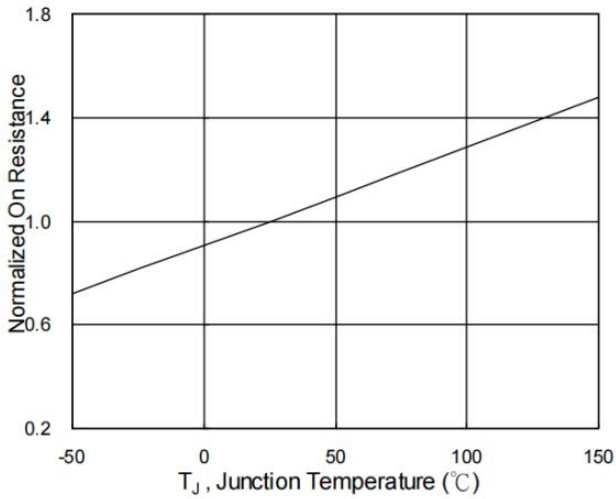


Fig.6 Normalized R_{DSON} vs T_J

20V N+P-Channel Enhancement Mode MOSFET

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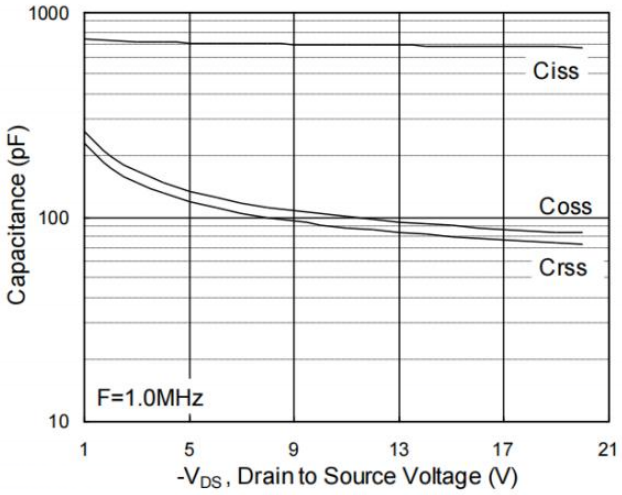


Fig.7 Capacitance

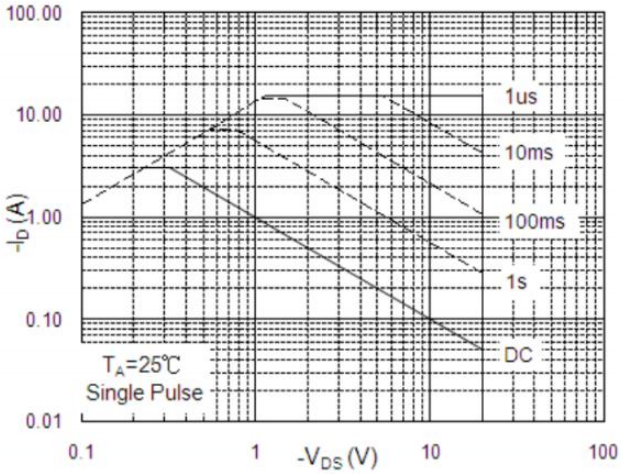


Fig.8 Safe Operating Area

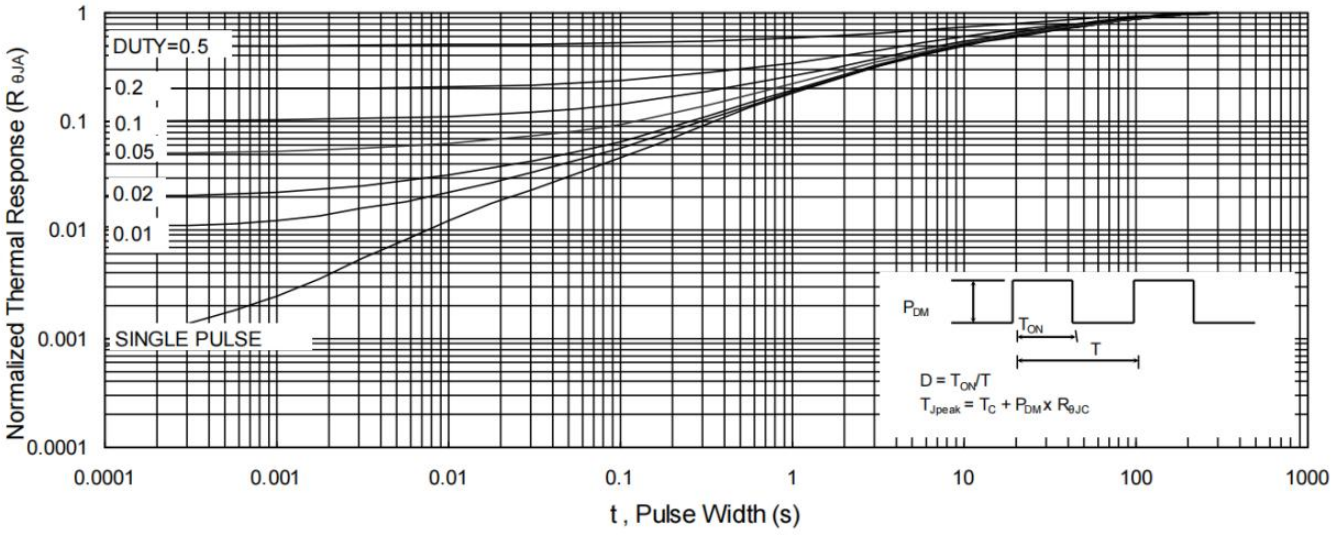


Fig.9 Normalized Maximum Transient Thermal Impedance

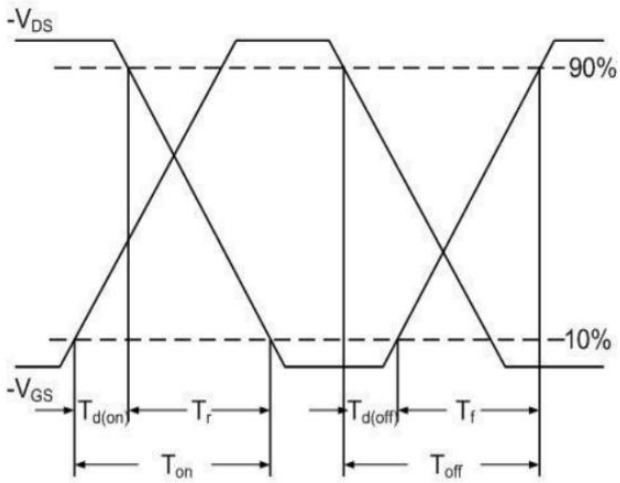


Fig.10 Switching Time Waveform

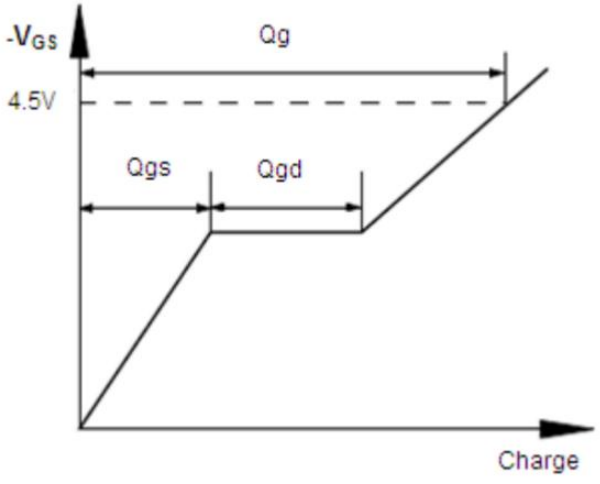
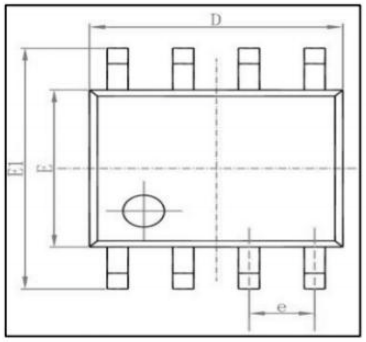
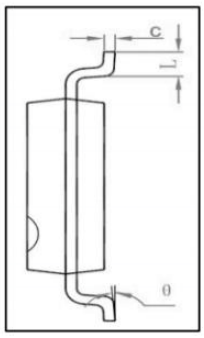


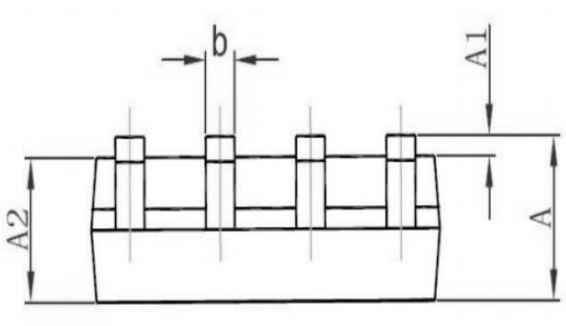
Fig.11 Gate Charge Waveform

20V N+P-Channel Enhancement Mode MOSFET

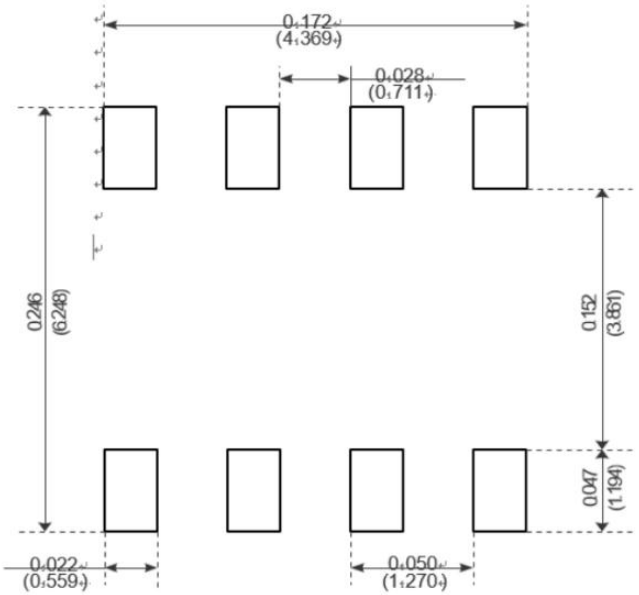
Package Mechanical Data-SOP-8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

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