

EVVOSEMI[®]

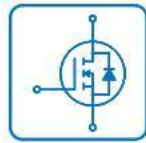
THINK CHANGE DO



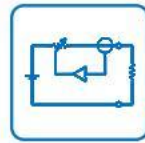
ESD



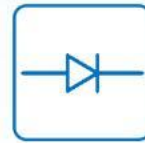
TVS



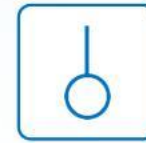
MOS



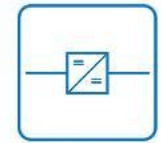
LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRFS4410Z
▶ Overseas	Part Number	IRFS4410Z
▶ Equivalent	Part Number	IRFS4410Z

EV is the abbreviation of name EVVO

General Description

IRFS4410Z use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

Features

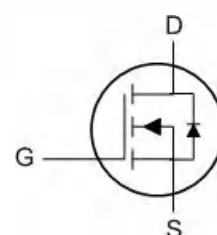
Low $R_{DS(on)}$ & FOM
 Extremely low switching loss
 Excellent stability and uniformity or Invertors

100V N-SGT Enhancement Mode MOSFET

Applications

Consumer electronic power supply
 Motor control
 Synchronous-rectification
 Isolated DC
 Synchronous-rectification applications

TO-263-2L Pin Configuration



Absolute Maximum Ratings at $T_J=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	80	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D, pulse}$	180	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	125	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	100	mJ
Operation and storage temperature	T_{stg}, T_J	-55 to 150	$^\circ\text{C}$
Thermal resistance, junction-case	$R_{\theta JC}$	1	$^\circ\text{C/W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	$^\circ\text{C/W}$

100V N-SGT Enhancement Mode MOSFET
Electrical Characteristics at $T_j=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BVDSS	100			V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		8	10	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=10\text{ A}$
Drain-source on-state resistance	$R_{DS(ON)}$		10	12	$\text{m}\Omega$	$V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$
Gate-source leakage current	IGSS			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	IDSS			1	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	Ciss		2604		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	Coss		361.2		pF	
Reverse transfer capacitance	Crss		6.5		pF	
Turn-on delay time	td(on)		20.6		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2.2\text{ }\Omega$, $I_D=25\text{ A}$
Rise time	t_r		5		ns	
Turn-off delay time	td(off)		51.8		ns	
Fall time	t_f		9		ns	
Total gate charge	Q_g		49.9		nC	$I_D=25\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$
Gate-source charge	Q_{gs}		6.5		nC	
Gate-drain charge	Q_{gd}		12.4		nC	
Gate plateau voltage	$V_{plateau}$		3.4		V	
Diode forward current	I_S			60		$V_{GS}<V_{th}$
Pulsed source current	ISP			180	A	
Diode forward voltage	VSD			1.3	V	$I_S=12\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	trr		60.4		ns	$I_S=12\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		106.1		nC	
Peak reverse recovery current	Irrm		3		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^{\circ}\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^{\circ}\text{C}$.

Electrical Characteristics Diagrams

100V N-SGT Enhancement Mode MOSFET

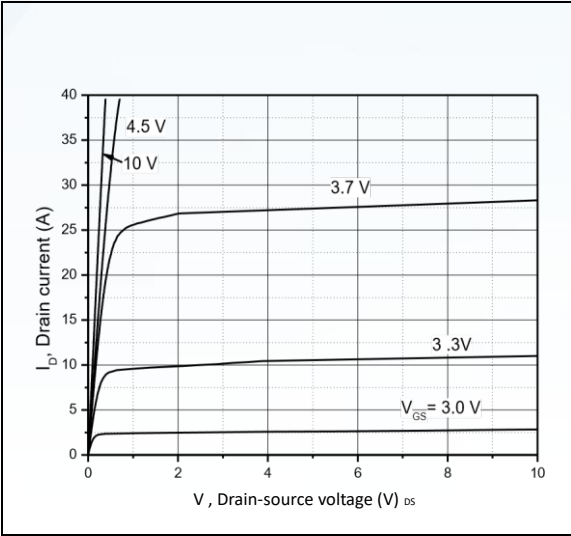


Figure 1, Typ. output characteristics

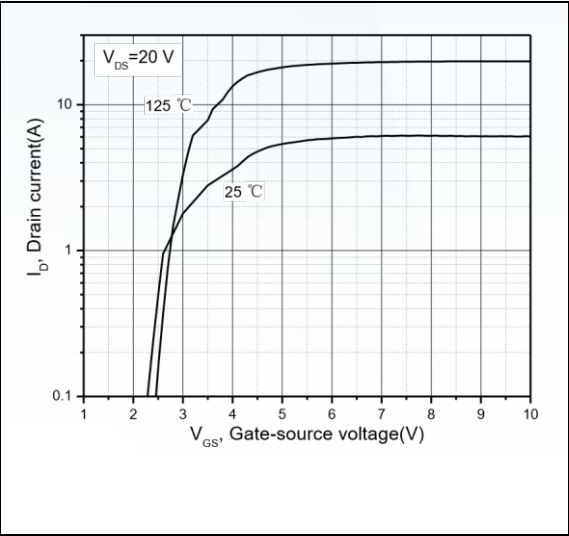


Figure 2, Typ. transfer characteristics

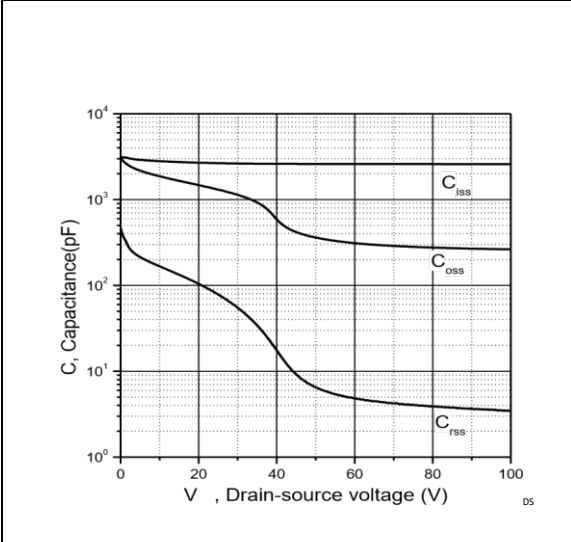


Figure 3, Typ. capacitances

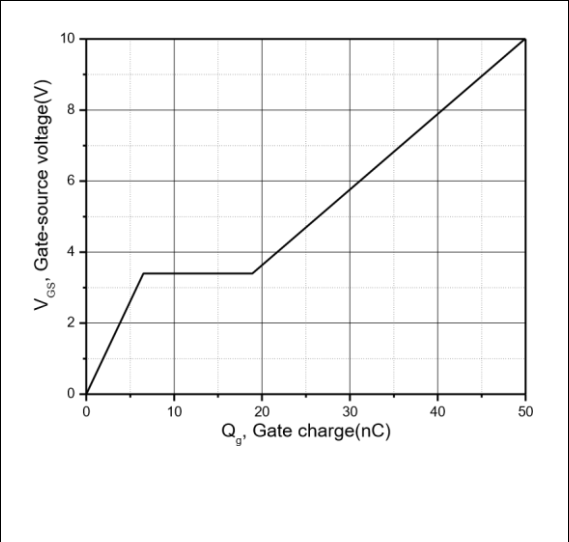


Figure 4, Typ. gate charge

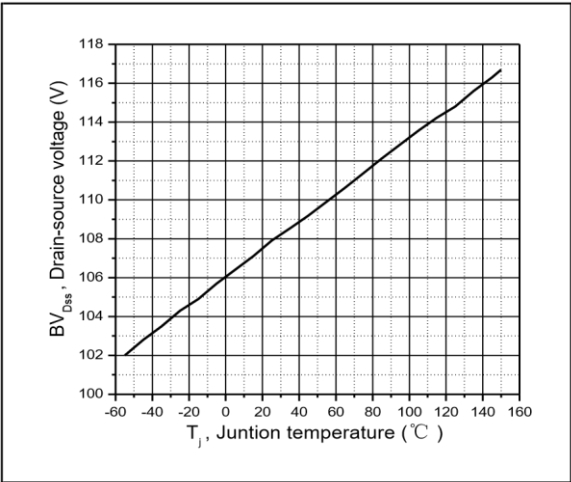


Figure 5, Drain-source breakdown voltage

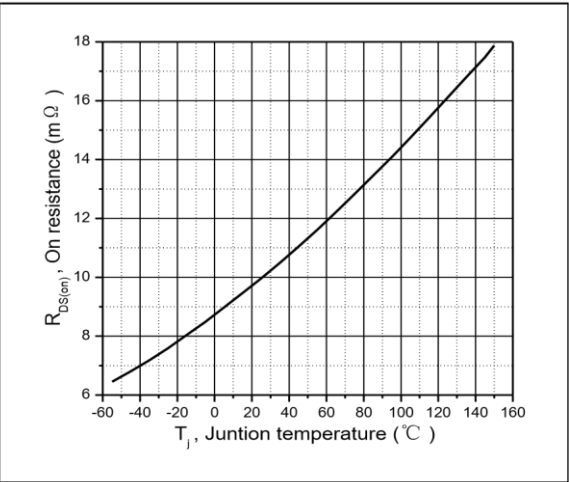


Figure 6, Drain-source on-state resistance

100V N-SGT Enhancement Mode MOSFET

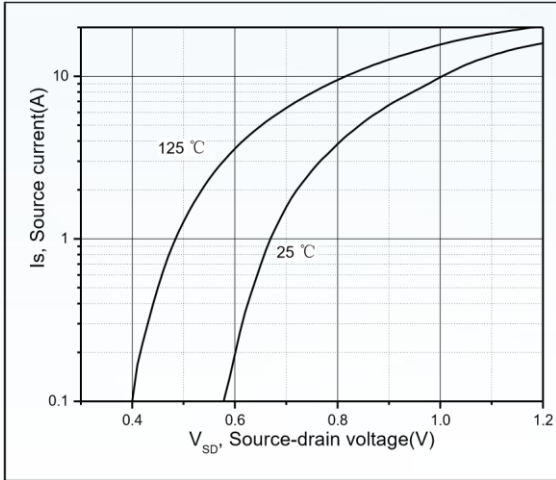


Figure 7, Forward characteristic of body diode

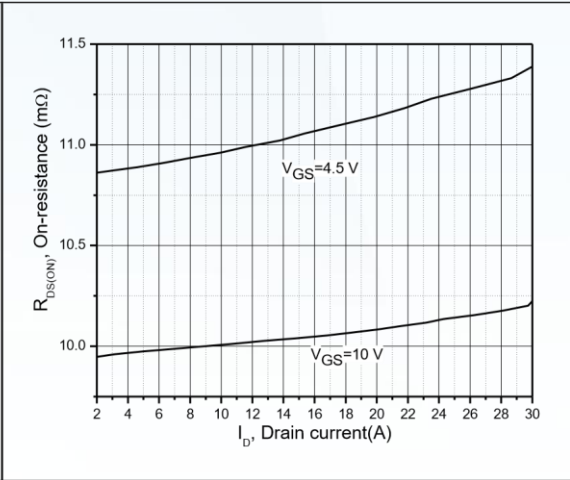


Figure 8, Drain-source on-state resistance

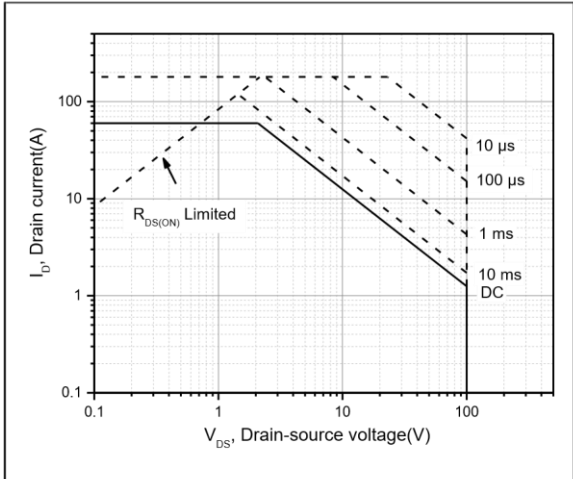


Figure 9, Safe operation area $T_C=25\text{ }^{\circ}\text{C}$

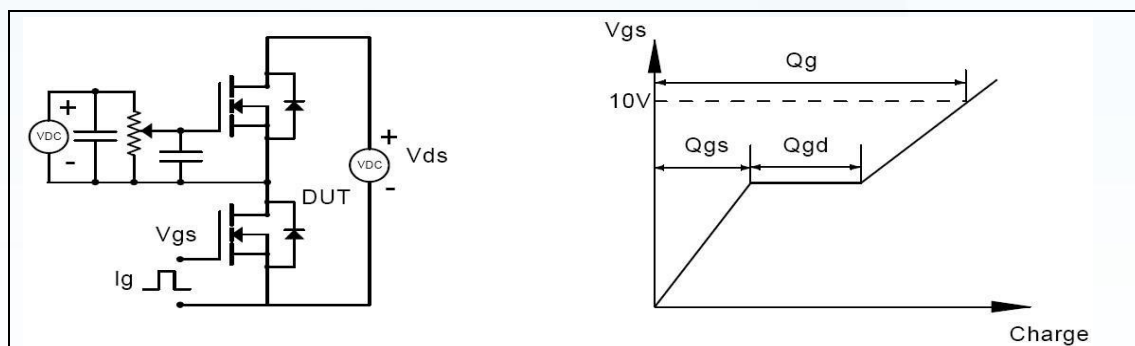
100V N-SGT Enhancement Mode MOSFET
Test circuits and waveforms


Figure 1, Gate charge test circuit & waveform

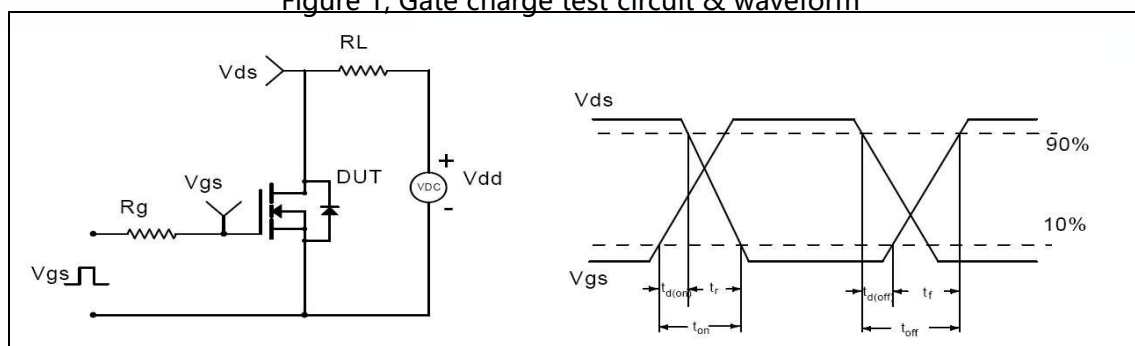


Figure 2, Switching time test circuit & waveforms

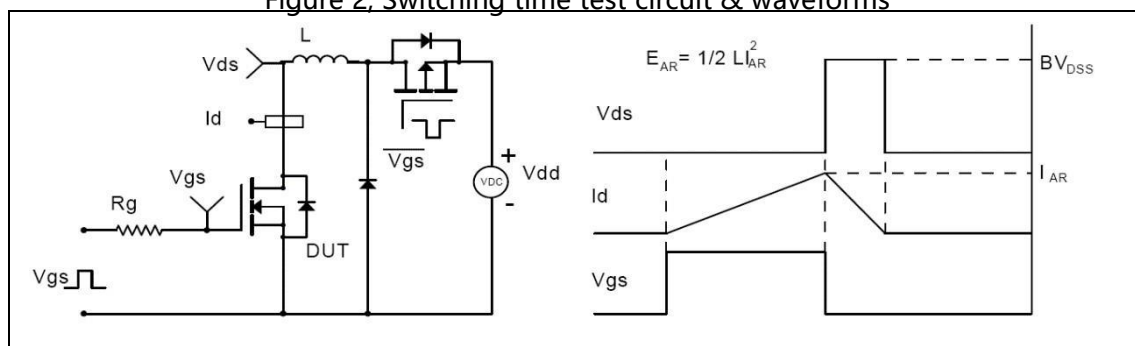


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

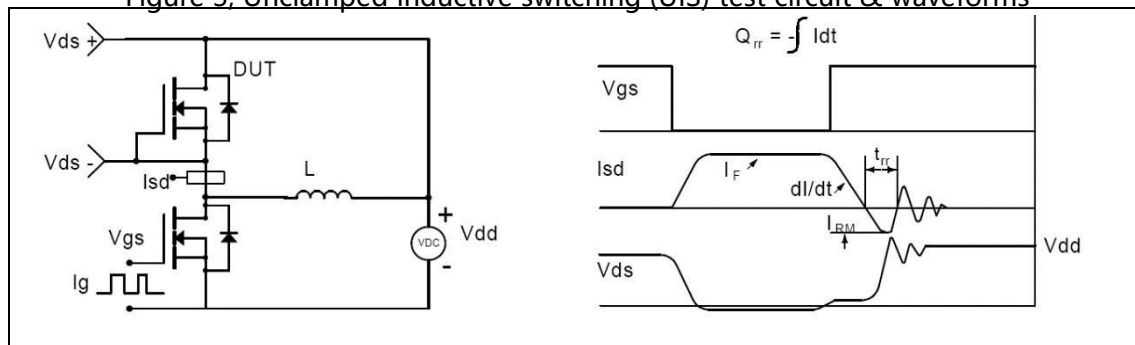
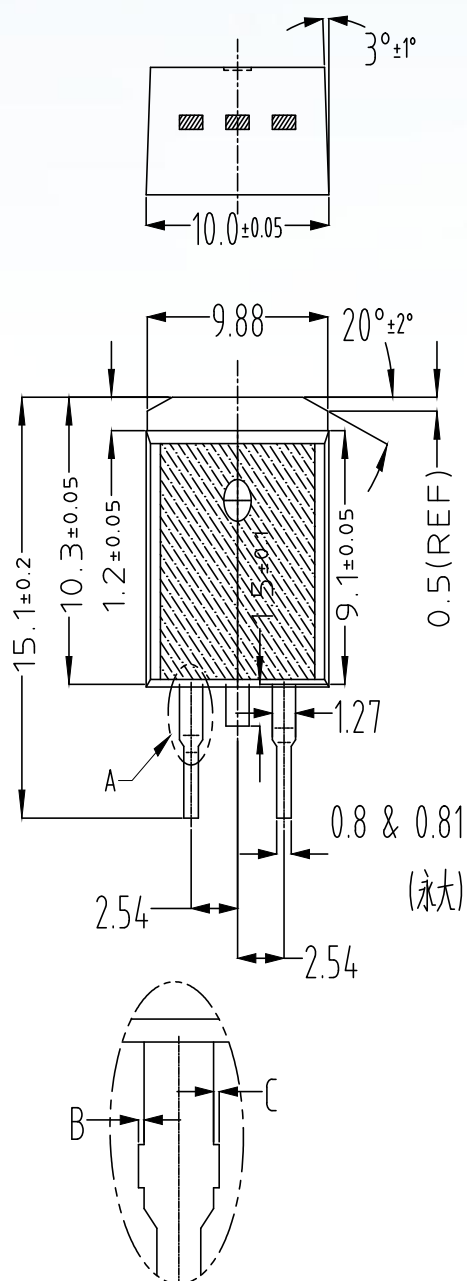


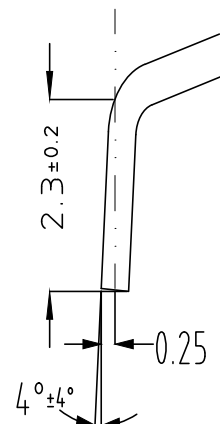
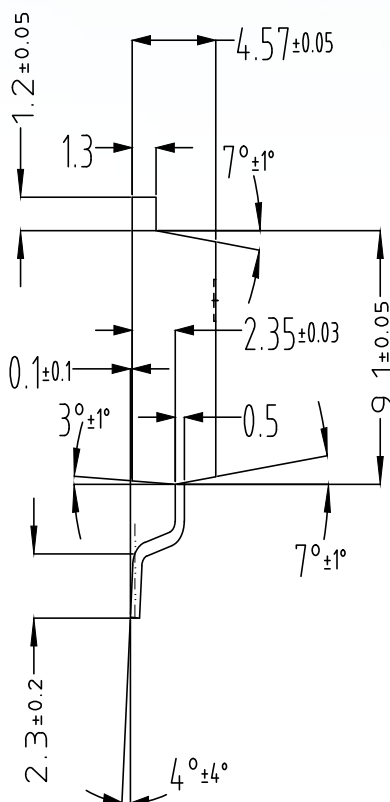
Figure 4, Diode reverse recovery test circuit & waveforms

100V N-SGT Enhancement Mode MOSFET
TO-263 Package Outline Dimensions

Package Outline Dimensions (Units: mm)



$$0 < B, C < 0.076$$



Disclaimer

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