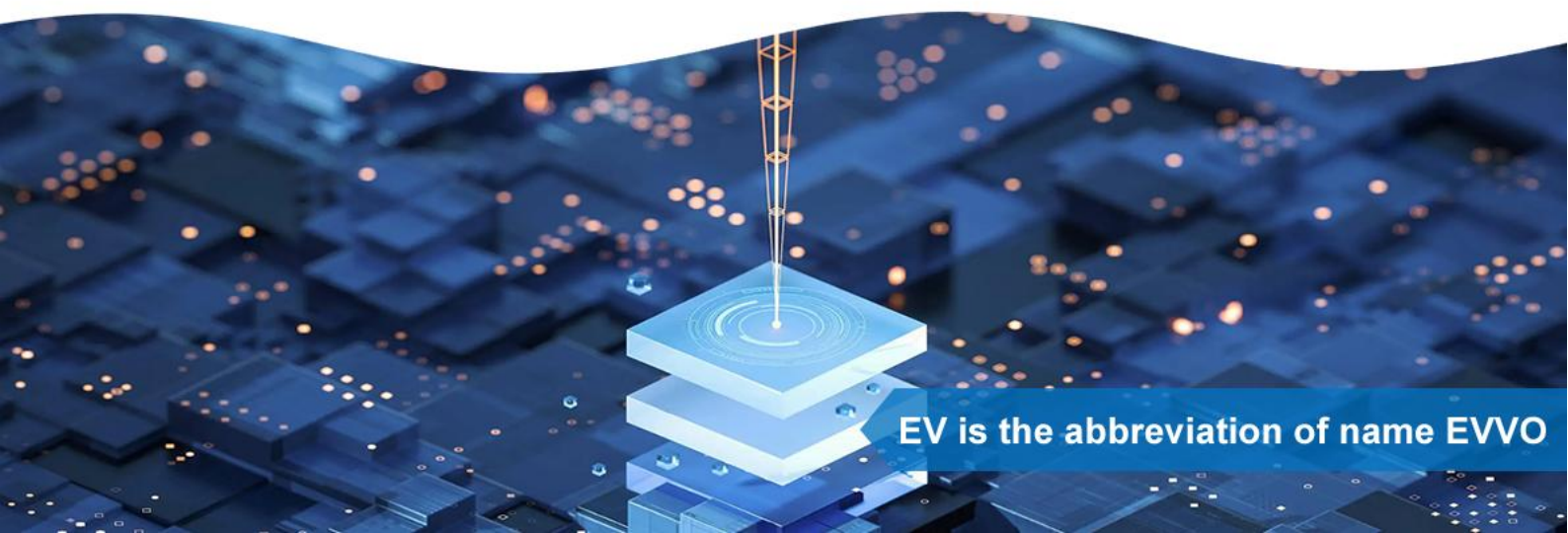
EVVOSEMI®

THINK CHANGE DO

ESD TVS MOS LDO Diode Sensor DC-DC

# Product Specification

| | |
|---|---|
| Domestic Part Number | BSZ146N10LS5 |
| Overseas Part Number | BSZ146N10LS5 |
| Equivalent Part Number | BSZ146N10LS5 |



# 100V N-SGT Enhancement Mode MOSFET

## General Description

BSZ146N10LS5 use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

## Features

Low RDS(on) & FOM

Extremely low switching loss

Excellent stability and uniformity or Invertors

## Applications

Consumer electronic power supply

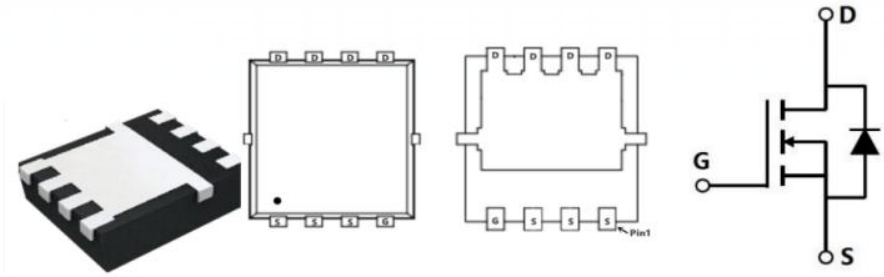
Motor control

Synchronous-rectification

Isolated DC

Synchronous-rectification applications

## PDFN3*3-8L Pin Configuration




## Absolute Maximum Ratings at $T_j$=25℃ unless otherwise noted

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain source voltage | $V_{DS}$ | 100 | V |
| Gate source voltage | $V_{GS}$ | ±20 | V |
| Continuous drain current[1], $T_C$=25 ℃ | $I_D$ | 68 | A |
| Pulsed drain current[2], $T_C$=25 ℃ | $I_{D,\ pulse}$ | 180 | A |
| Power dissipation[3], $T_C$=25 ℃ | $P_D$ | 125 | W |
| Single pulsed avalanche energy[5] | $E_{AS}$ | 100 | mJ |
| Operation and storage temperature | $T_{stg}$, $T_j$ | -55 to 150 | ℃ |
| Thermal resistance, junction-case | $R_{\theta JC}$ | 1 | ℃/W |
| Thermal resistance, junction-ambient[4] | $R_{\theta JA}$ | 62 | ℃/W |

**100V N-SGT Enhancement Mode MOSFET**

## Electrical Characteristics at $T_j$=25 ℃ unless otherwise specified

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test condition |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | BVDSS | 100 | | | V | $V_{GS}$=0 V, $I_D$=250 μA |
| Gate threshold voltage | VGS(th) | 1.2 | 2.0 | 2.5 | V | $V_{DS}$=$V_{GS}$, $I_D$=250 μA |
| Drain-source on-state resistance | RDS(ON) | | 6.4 | 7.7 | mΩ | $V_{GS}$=10 V, $I_D$=20 A |
| Drain-source on-state resistance | RDS(ON) | | 9.3 | 11.6 | mΩ | $V_{GS}$=4.5 V, $I_D$=15 A |
| Gate-source leakage current | IGSS | | | 100 | nA | $V_{GS}$=20 V |
| | | | | -100 | | $V_{GS}$=-20 V |
| Drain-source leakage current | IDSS | | | 1 | μA | $V_{DS}$=80 V, $V_{GS}$=0 V |
| Input capacitance | Ciss | | 2604 | | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, f=1 MHz |
| Output capacitance | Coss | | 361.2 | | pF | |
| Reverse transfer capacitance | Crss | | 6.5 | | pF | |
| Turn-on delay time | td(on) | | 20.6 | | ns | $V_{GS}$=10 V, $V_{DS}$=50 V, $R_G$=2.2 Ω, $I_D$=25 A |
| Rise time | $t_r$ | | 5 | | ns | |
| Turn-off delay time | td(off) | | 51.8 | | ns | |
| Fall time | $t_f$ | | 9 | | ns | |
| Total gate charge | $Q_g$ | | 49.9 | | nC | $I_D$=25 A, $V_{DS}$=50 V, $V_{GS}$=10 V |
| Gate-source charge | $Q_{gs}$ | | 6.5 | | nC | |
| Gate-drain charge | Qgd | | 12.4 | | nC | |
| Gate plateau voltage | Vplateau | | 3.4 | | V | |
| Diode forward current | $I_S$ | | | 60 | | VGS<Vth |
| Pulsed source current | ISP | | | 180 | A | |
| Diode forward voltage | VSD | | | 1.3 | V | $I_S$=12 A, $V_{GS}$=0 V |
| Reverse recovery time | trr | | 60.4 | | ns | $I_S$=12 A, di/dt=100 A/μs |
| Reverse recovery charge | $Q_{rr}$ | | 106.1 | | nC | |
| Peak reverse recovery current | Irrm | | 3 | | A | |

## Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a$=25 ℃.
5) $V_{DD}$=50 V, $R_G$=25 Ω, L=0.3 mH, starting $T_j$=25 ℃.

## Electrical Characteristics Diagrams

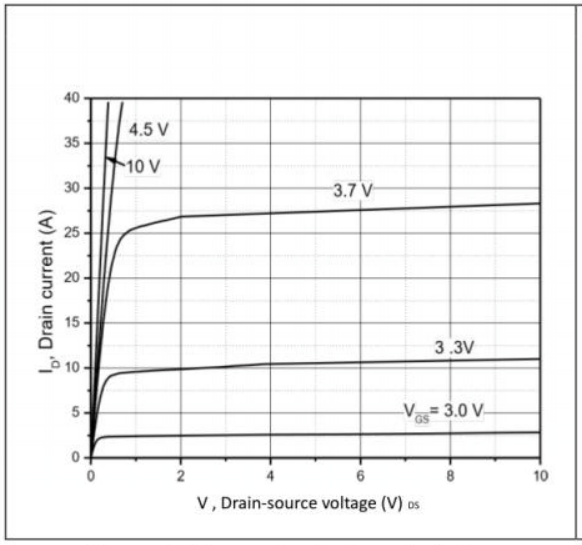



Figure 1, Typ. output characteristics

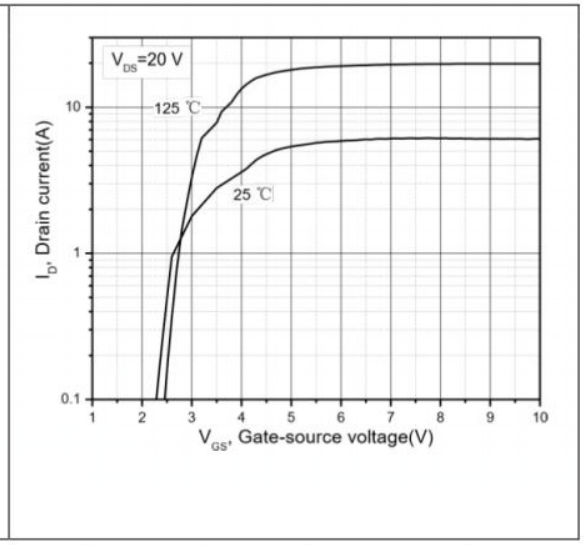



Figure 2, Typ. transfer characteristics

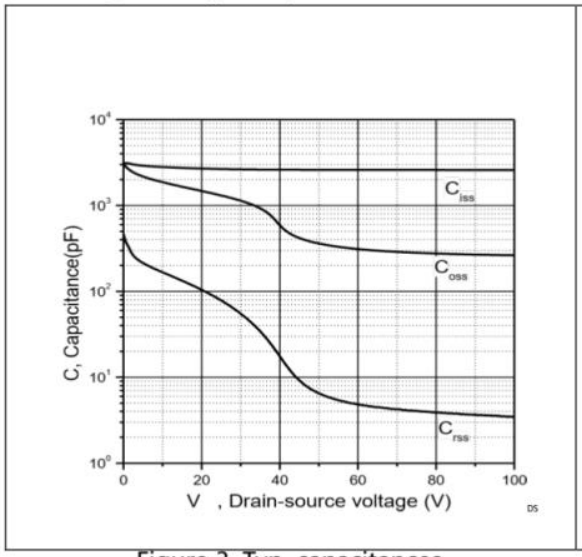



Figure 3, Typ. capacitances

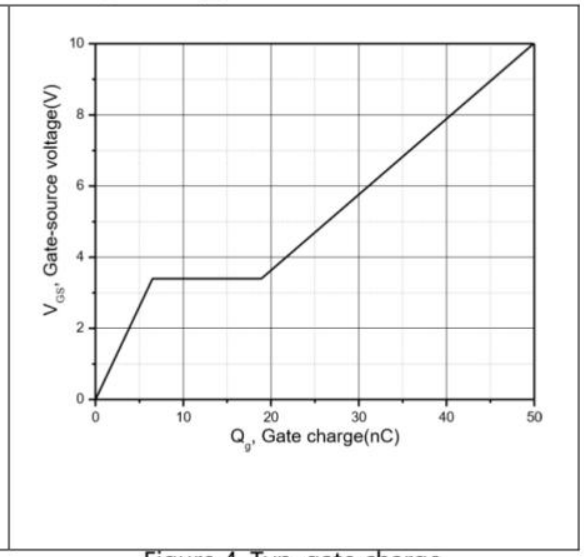



Figure 4, Typ. gate charge

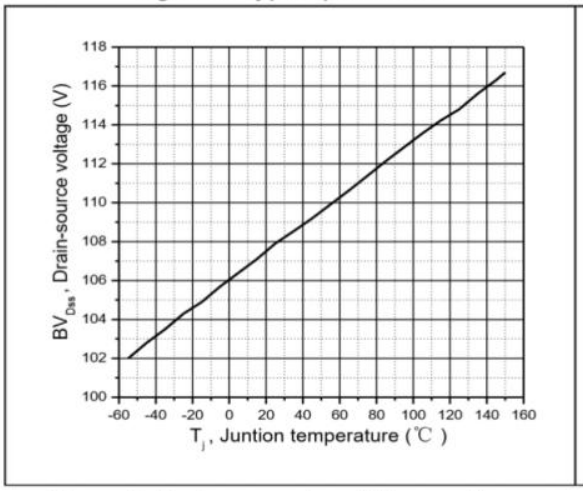



Figure 5, Drain-source breakdown voltage

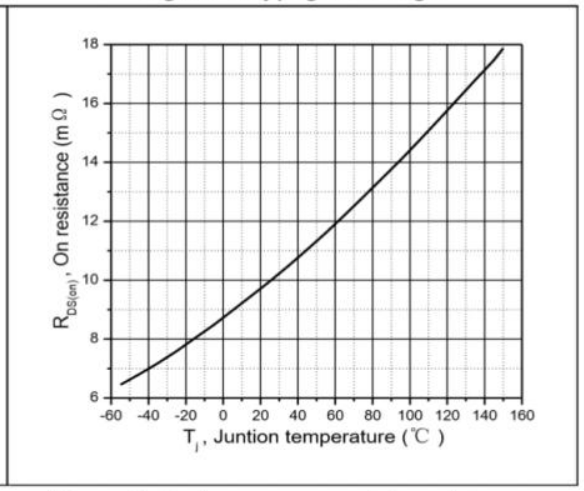



Figure 6, Drain-source on-state resistance

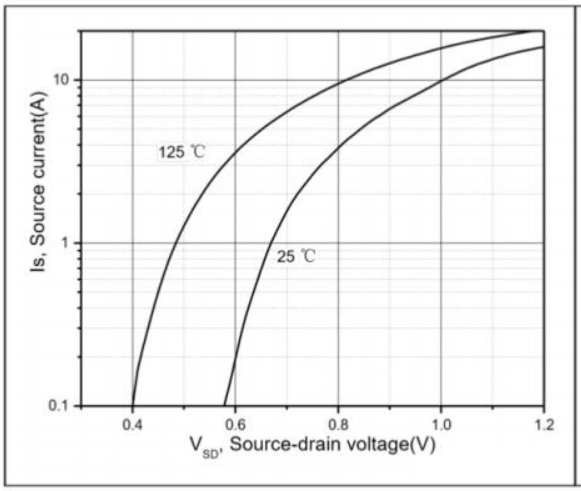



Figure 7, Forward characteristic of body diode

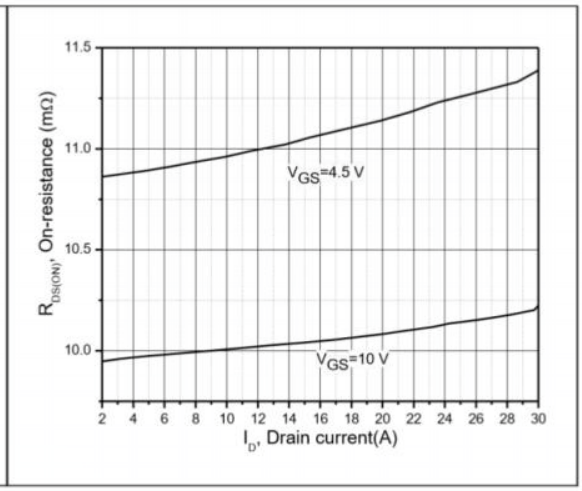



Figure 8, Drain-source on-state resistance

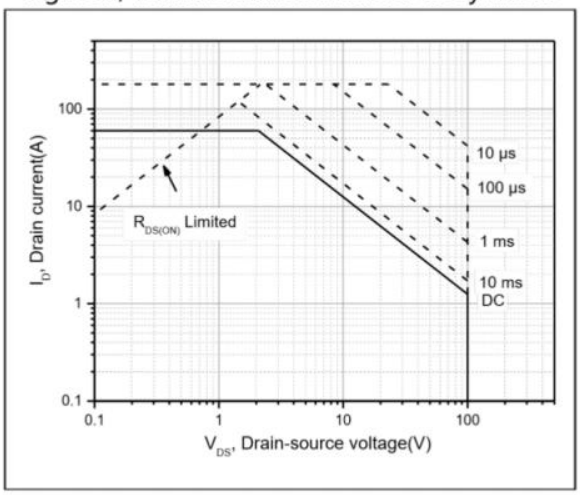



Figure 9, Safe operation area $T_C$=25 ℃

## Test circuits and waveforms

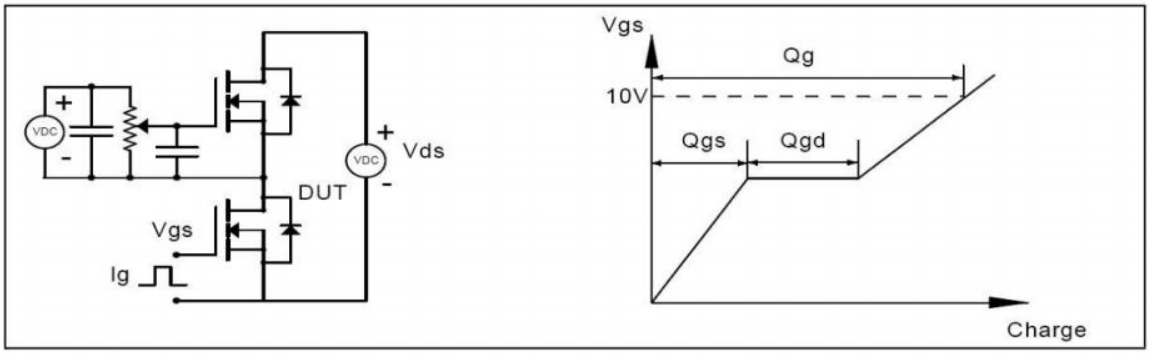



Figure 1, Gate charge test circuit & waveform

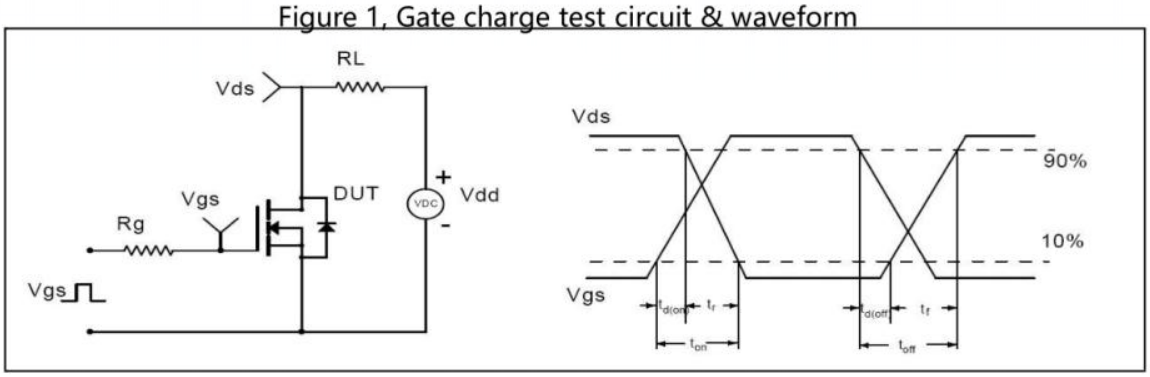



Figure 2, Switching time test circuit & waveforms

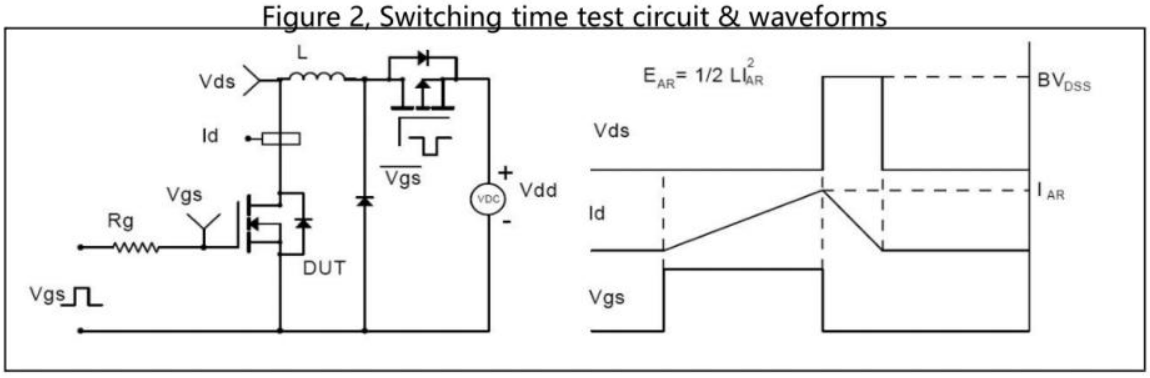



Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

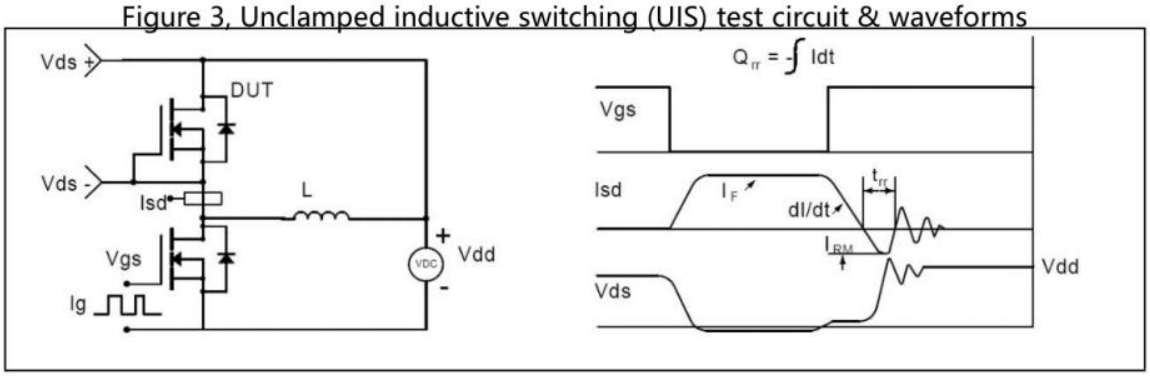
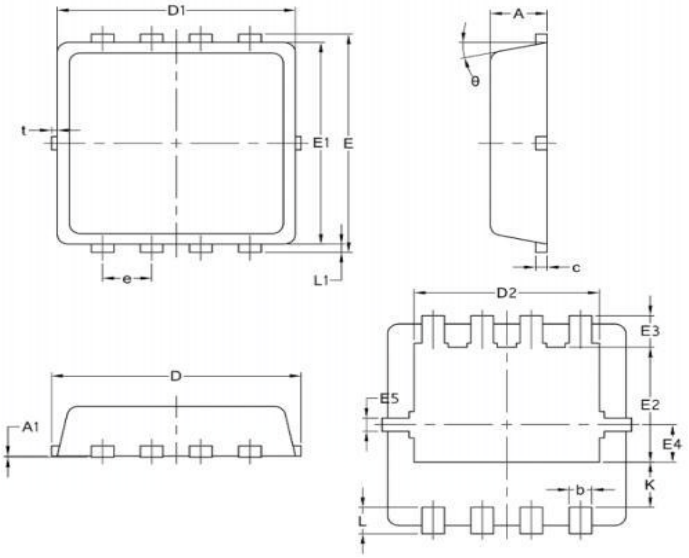



Figure 4, Diode reverse recovery test circuit & waveforms

## Package Mechanical Data-DFN3*3-8L-Jcw Single




| Symbol | Common | | |
|---|---|---|---|
| | mm | | |
| | Mim | Nom | Max |
| A | 0.70 | 0.75 | 0.85 |
| A1 | / | / | 0.05 |
| b | 0.20 | 0.30 | 0.40 |
| c | 0.10 | 0.152 | 0.25 |
| D | 3.15 | 3.30 | 3.45 |
| D1 | 3.00 | 3.15 | 3.25 |
| D2 | 2.29 | 2.45 | 2.65 |
| E | 3.15 | 3.30 | 3.45 |
| E1 | 2.90 | 3.05 | 3.20 |
| E2 | 1.54 | 1.74 | 1.94 |
| E3 | 0.28 | 0.48 | 0.65 |
| E4 | 0.37 | 0.57 | 0.77 |
| E5 | 0.10 | 0.20 | 0.30 |
| e | 0.60 | 0.65 | 0.70 |
| K | 0.59 | 0.69 | 0.89 |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.06 | 0.125 | 0.20 |
| t | 0 | 0.075 | 0.13 |
| Φ | 10 | 12 | 14 |

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