

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	BSC057N08N
▶ Overseas	Part Number	BSC057N08N
▶ Equivalent	Part Number	BSC057N08N

EV is the abbreviation of name EVVO

80V N-Channel Enhancement Mode MOSFET

General Description

BSC057N08N use advanced MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications

General Features

$V_{DS} = 80V$ $I_D = 92A$

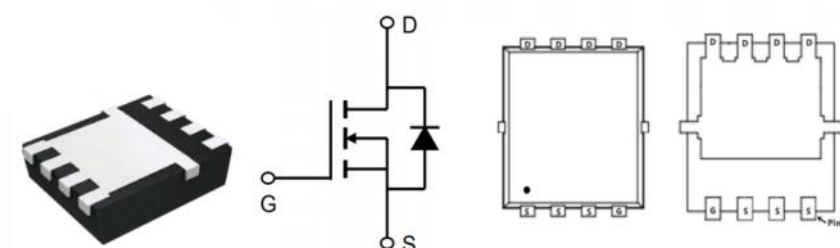
$R_{DS(ON)} < 7.5m\Omega$ @ $V_{GS}=10V$

Low $R_{DS(on)}$ & FOM

Extremely low switching loss

Excellent stability and uniformity or Invertors

PDFN5*6-8L Pin Configuration



Package Marking and Ordering Information

Product ID	Package	Marking	QTY(PCS)	Packing method
BSC057N08N	PDFN5*6-8L	T65HND	5000	Reel

Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	80	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾	I_D	92	A
Pulsed drain current ²⁾	$I_{D, pulse}$	400	A
Power dissipation ³⁾	P_D	148	W
Single pulsed avalanche energy ⁵⁾	EAS	205	mJ
Operation and storage temperature	Tstg, T_j	-55 to 150	$^\circ\text{C}$
Thermal resistance, junction-case	$R_{\theta JC}$	0.84	$^\circ\text{C/W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	75	$^\circ\text{C/W}$

80V N-Channel Enhancement Mode MOSFET
Electrical Characteristics at $T_j=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	80	90		V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	2		4	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		6.5	7.5	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=12\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		3600		pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		402		pF	
Reverse transfer capacitance	C_{rss}		366		pF	
Turn-on delay time	$t_{d(on)}$		22.0		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2\text{ }\Omega$, $I_D=25\text{ A}$
Rise time	t_r		21.5		ns	
Turn-off delay time	$t_{d(off)}$		62.7		ns	
Fall time	t_f		61.4		ns	
Total gate charge	Q_g		52.6		nC	$I_D=25\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$
Gate-source charge	Q_{gs}		14.7		nC	
Gate-drain charge	Q_{gd}		7.5		nC	
Gate plateau voltage	$V_{plateau}$		3.8		V	
Diode forward current	I_S			100	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			300		
Diode forward voltage	V_{SD}			1.3	V	$I_S=12\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		75.0		ns	$I_S=25\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		159.8		nC	
Peak reverse recovery current	I_{rrm}		3.4		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^{\circ}\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^{\circ}\text{C}$.

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Electrical Characteristics Diagrams

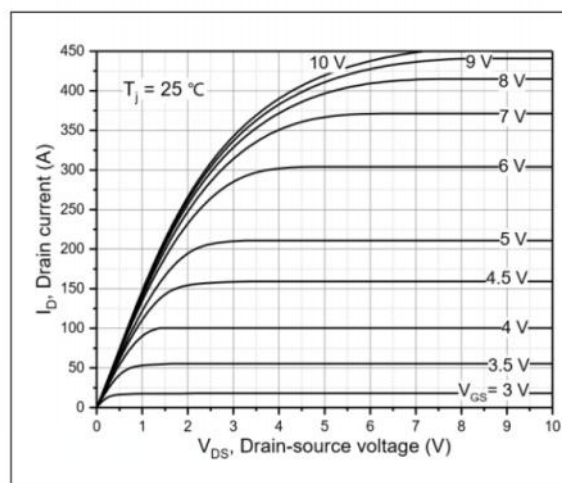


Figure 1, Typ. output characteristics

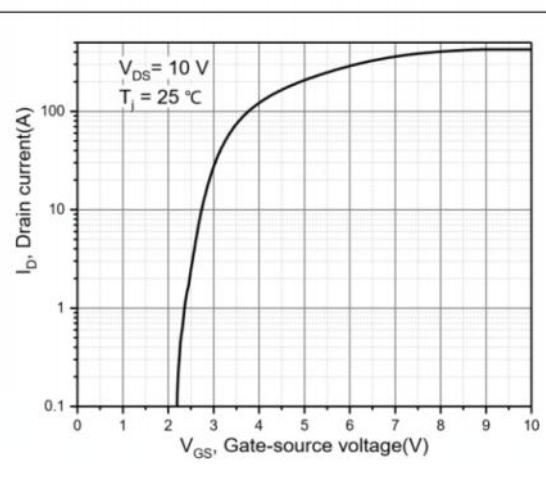


Figure 2, Typ. transfer characteristics

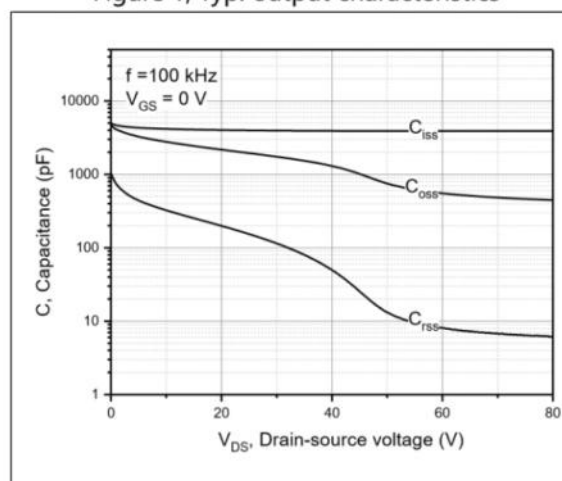


Figure 3, Typ. capacitances

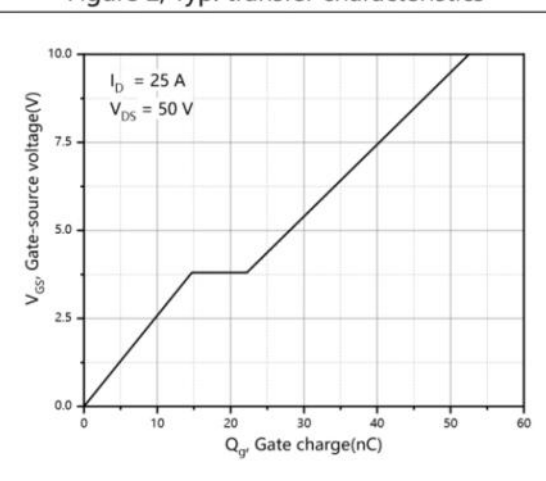


Figure 4, Typ. gate charge

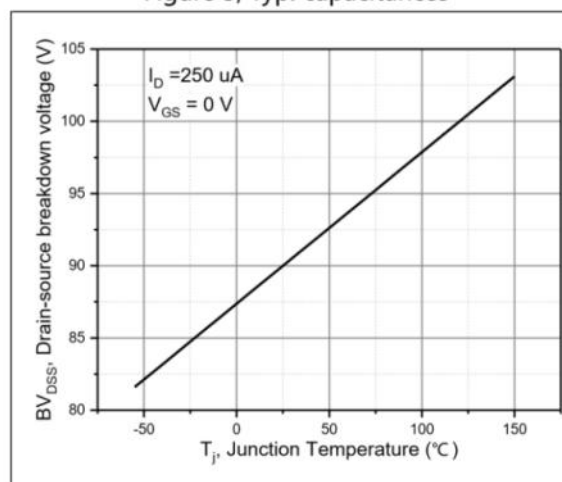


Figure 5, Drain-source breakdown voltage

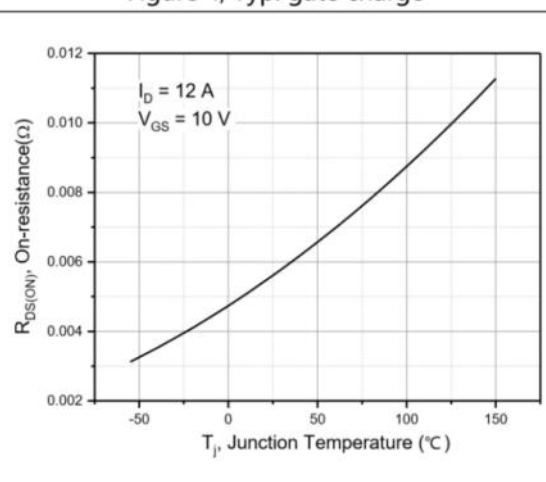


Figure 6, Drain-source on-state resistance

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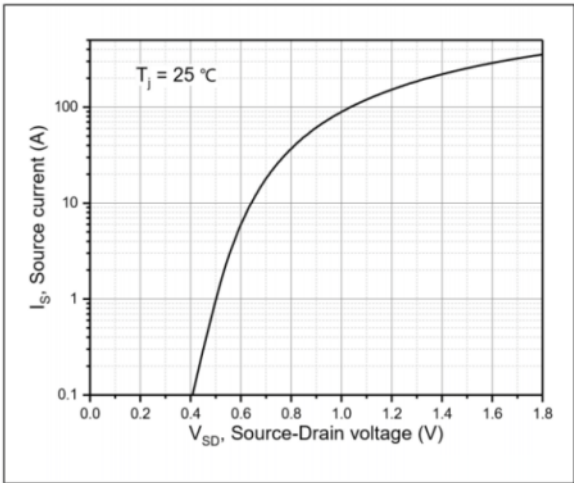


Figure 7, Forward characteristic of body diode

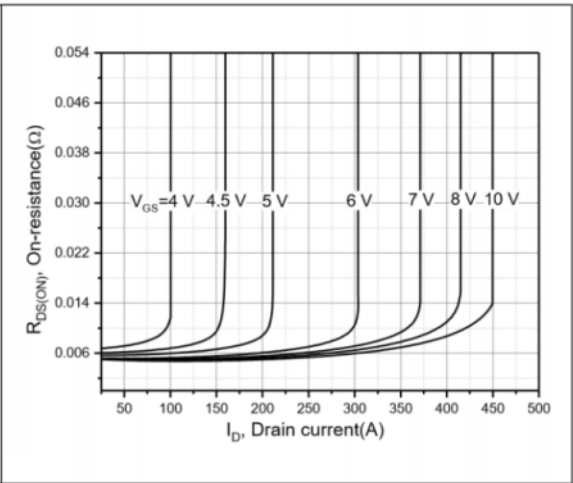


Figure 8, Drain-source on-state resistance

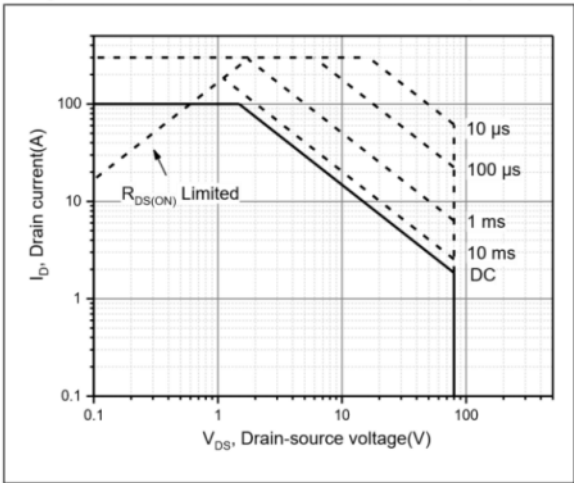


Figure 9, Safe operation area $T_C=25\text{ }^{\circ}\text{C}$

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Test circuits and waveforms

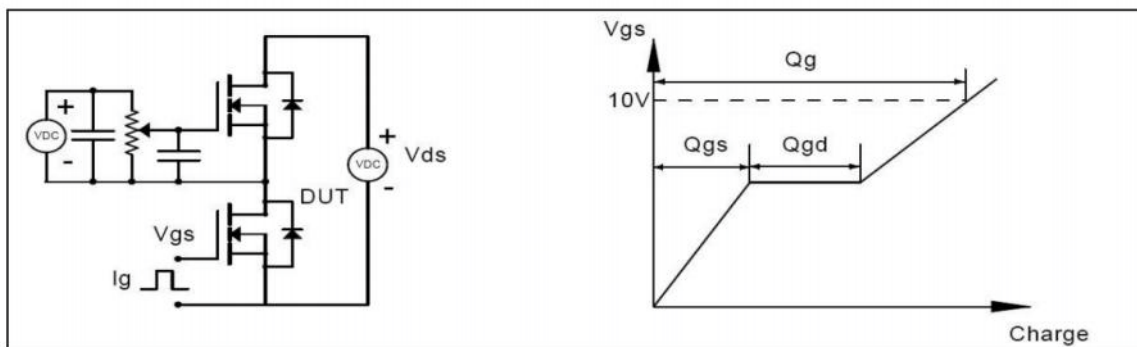


Figure 1, Gate charge test circuit & waveform

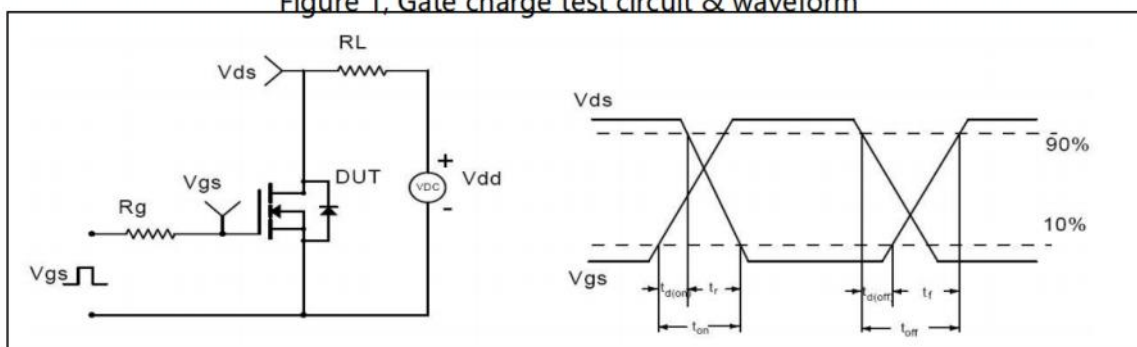


Figure 2, Switching time test circuit & waveforms

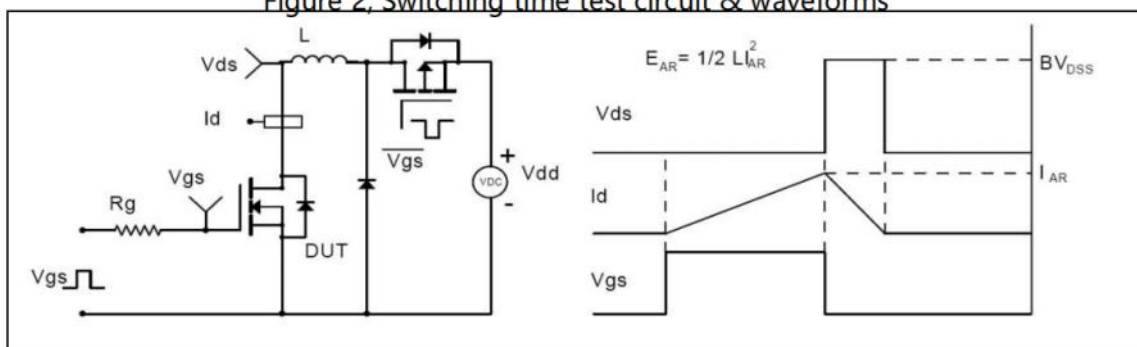


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

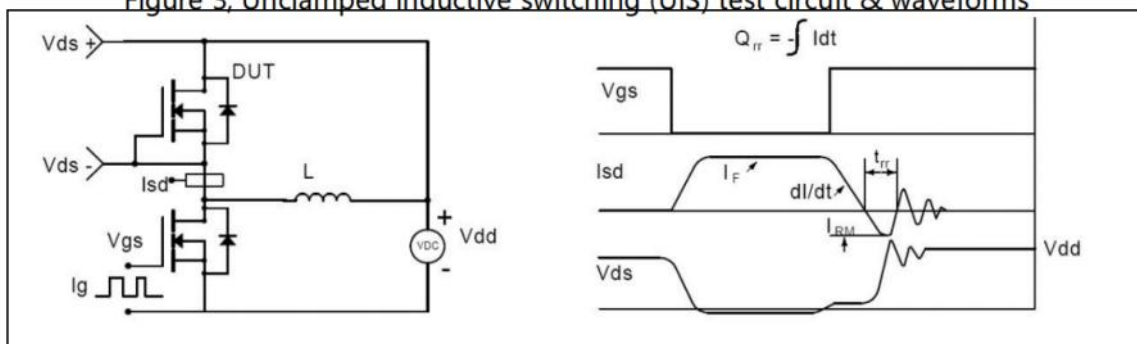
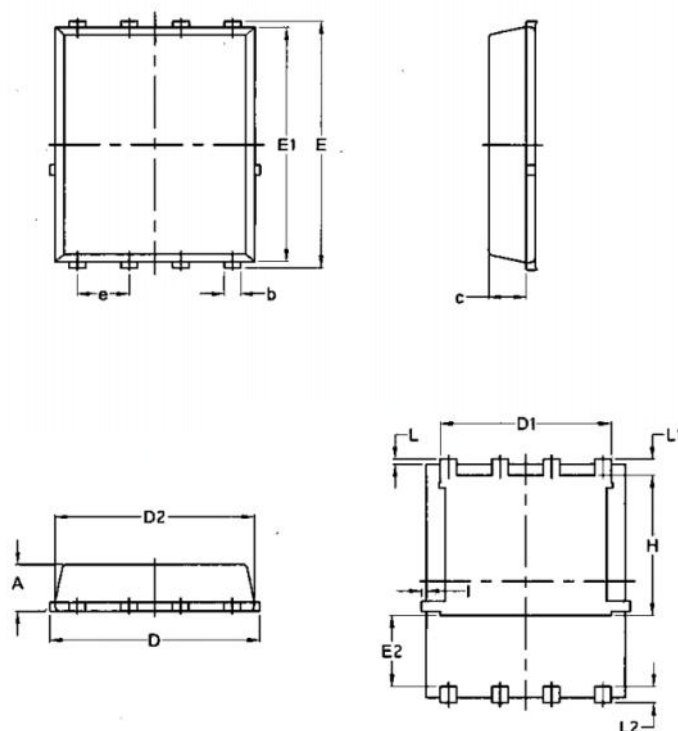


Figure 4, Diode reverse recovery test circuit & waveforms

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Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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