

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRL2505
▶ Overseas	Part Number	IRL2505
▶ Equivalent	Part Number	IRL2505

EV is the abbreviation of name EVVO

N-Channel Enhancement Mode Power MOSFET

Description

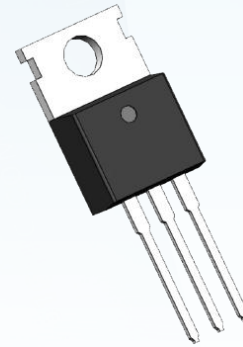
The IRL2505 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate Charge It can be used in a wide variety of applications.

Application

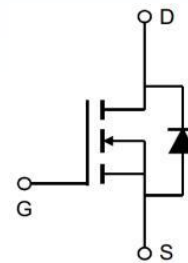
- ☐ Power switching application.
- ☐ Hard switched and high frequency circuits.
- ☐ Uninterruptible power supply.

Features

- ☐ $V_{DS} = 60V$, $I_D = 80A$
- ☐ $R_{DS(ON)} : 8m\Omega @ V_{GS}=10V$
- ☐ Low gate charge.
- ☐ Green device available.
- ☐ Advanced high cell density trench technology for ultra low on-resistance.
- ☐ Excellent package for good heat dissipation.



Marking and pin assignment



N-Channel MOSFET

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain- Source Voltage	60	V
V_{GS}	Gate Source Voltage	± 20	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current ¹	80	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current ¹	51	A
I_{DM}	Pulsed Drain Current ³	320	A
E_{AS}, E_{AR}	Avalanche Energy ⁵	18	mJ
I_{AS}, I_{AR}	Avalanche Current ⁵	19	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation ⁴	103	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to- Case ²	1.21	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ²	62	$^\circ\text{C/W}$

Electrical Characteristics (TC=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	---	60	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=10A$	---	8	10	mΩ
		$V_{GS}=4.5V, I_D=10A$	---	11	14	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1	2	3	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=60V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	μA
		$V_{DS}=48V, V_{GS}=0V, T_J=85^\circ C$	---	---	10	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	±100	nA
g_{FS}	Forward Transconductance	$V_{DS}=10V, I_D=10A$	---	20	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=30V, V_{GS}=10V, I_D=40A$	---	24	36	nC
Q_{gs}	Gate-Source Charge		---	1.9	3	
Q_{gd}	Gate-Drain Charge		---	5	7.5	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, I_{DS}=40A,$ $V_{GEN}=10V, R_G=6\Omega$	---	10	15	nS
T_r	Rise Time		---	23	35	
$T_{d(off)}$	Turn-Off Delay Time		---	27	41	
T_f	Fall Time		---	12	18	
C_{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1MHz$	---	950	1690	pF
C_{oss}	Output Capacitance		---	430	645	
C_{rss}	Reverse Transfer Capacitance		---	30	45	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$	---	---	80	A
I_{SM}	Pulsed Source Current		---	---	160	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_{SD}=10A, T_J=25^\circ C$	---	---	0.8	V
T_{rr}	Reverse Recovery Time	$I_S=10A, V_{GS}=10V,$ $di/dt=100A/\mu s, T_J=25^\circ C$	---	40	---	nS
Q_{rr}	Reverse Recovery Charge		---	40	---	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.
5. The EAS test condition is $V_{DD}=30V, V_{GS}=10V, L=0.1mH, I_{AS}=19A$

N-Ch 60V Fast Switching MOSFETs

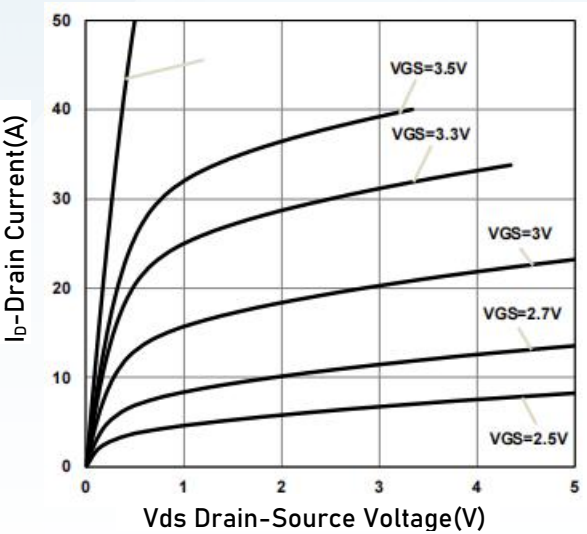


Fig.1 Typical Output Characteristics

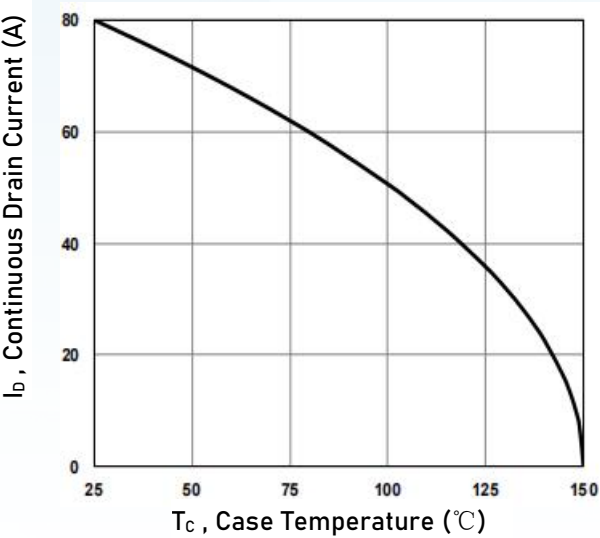


Fig.2 Drain Current

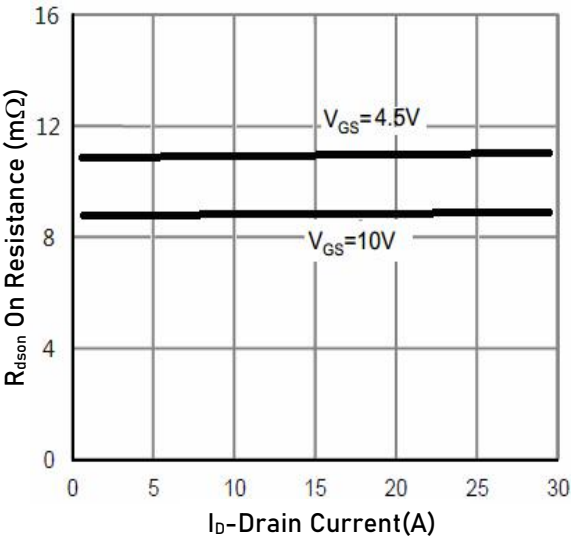


Fig.3 Drain-Source On Resistance

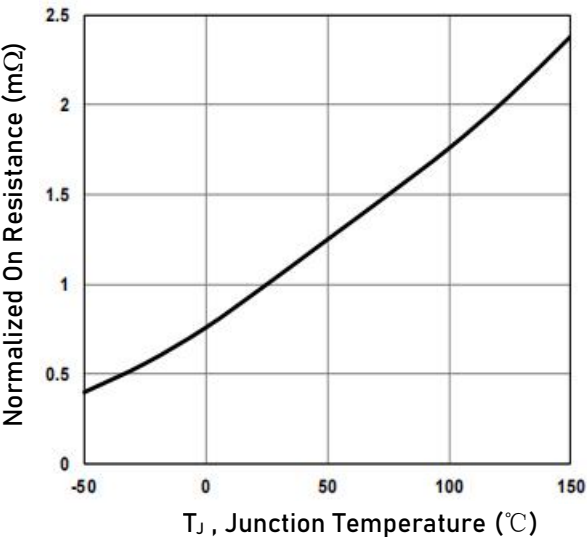


Fig.4 Normalized RDSON vs. T_J

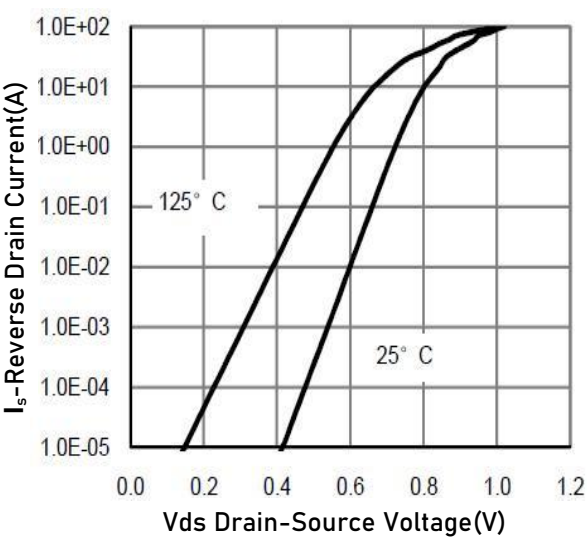


Fig.5 Forward Characteristics Of Reverse

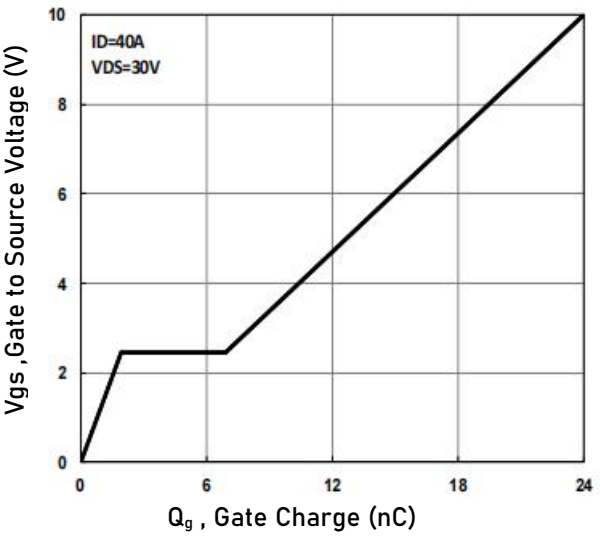


Fig.6 Gate-Charge Characteristics

N-Ch 60V Fast Switching MOSFETs

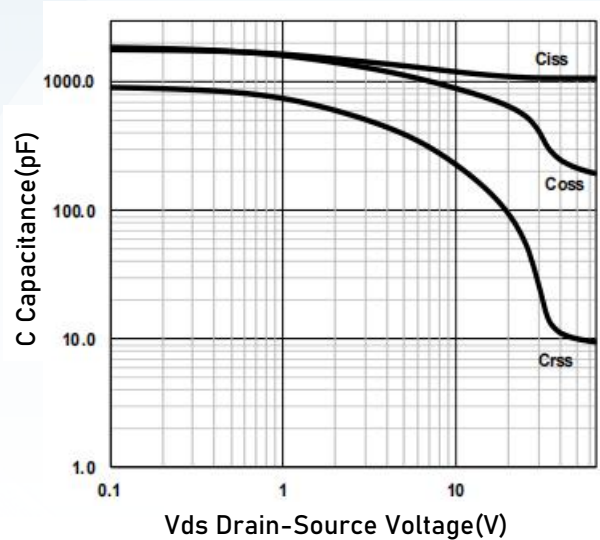


Fig.7 Capacitance

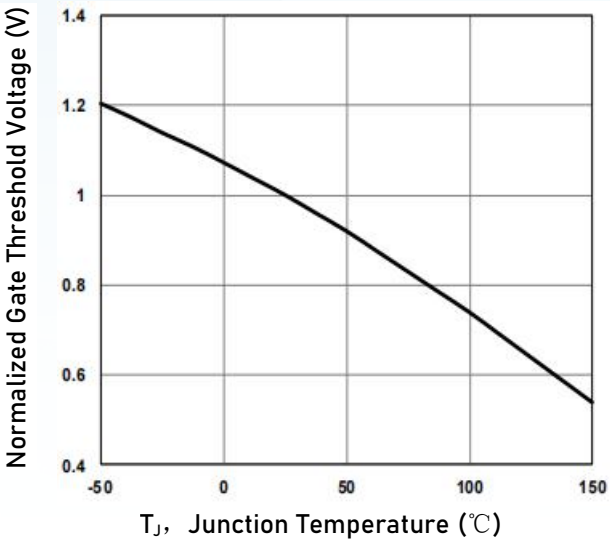


Fig.8 Normalized V_{th} vs. T_J

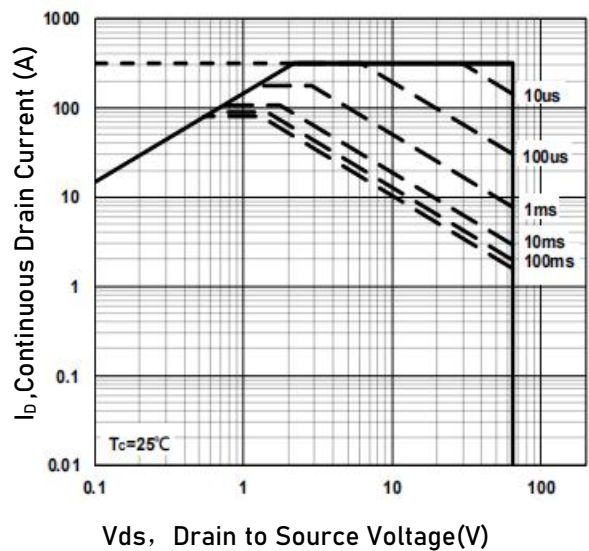


Fig.9 Safe Operating Area

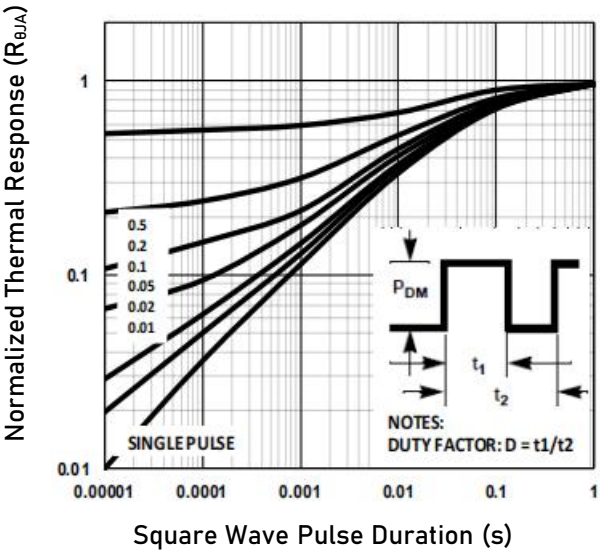
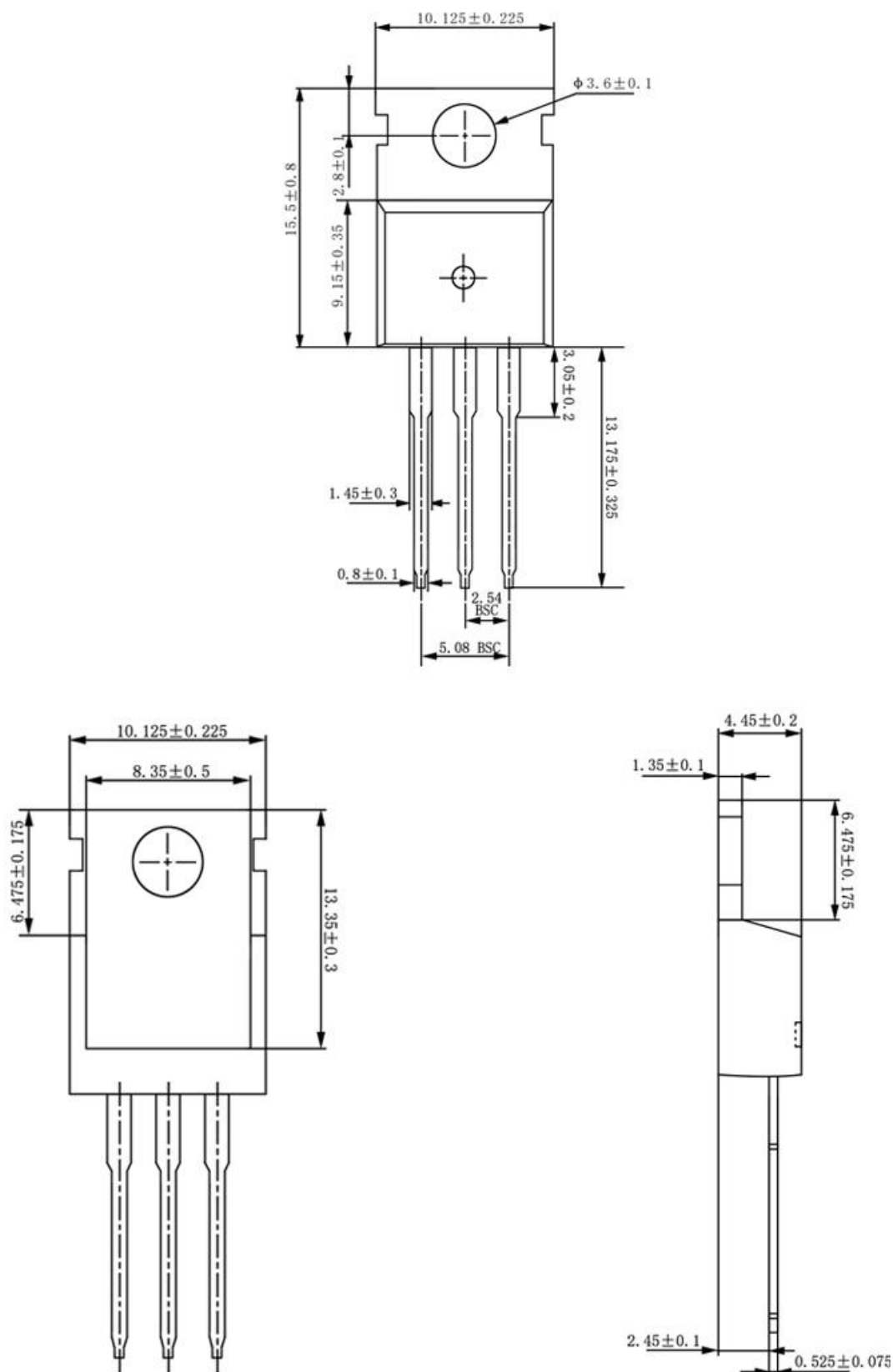


Fig.10 Transient Thermal Impedance

TO-220 Package Information



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