

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRFL024Z
▶ Overseas	Part Number	IRFL024Z
▶ Equivalent	Part Number	IRFL024Z

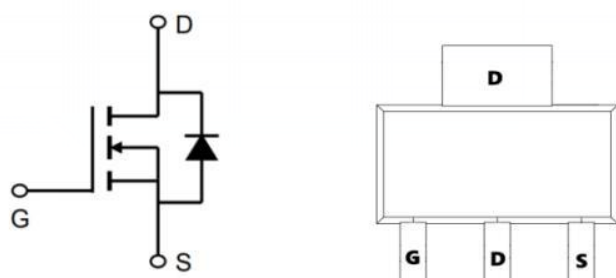
EV is the abbreviation of name EVVO

60V N-Channel Enhancement Mode MOSFET

Description

The IRFL024Z uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

SOT223-3L Pin Configuration



General Features

$V_{DS} = 60V$ $I_D = 50 A$

$R_{DS(ON)} < 17m\Omega$ @ $V_{GS}=10V$

$R_{DS(ON)} < 23m\Omega$ @ $V_{GS}=4.5V$

Application

Battery protection

Load switch

Uninterruptible power supply

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	50	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	10	A
I_{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	80	mJ
I_{AS}	Avalanche Current	40	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	41	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹ ($t \leq 10S$)	35	$^\circ C/W$
	Thermal Resistance Junction-ambient ¹ (Steady State)	55	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-case ¹	3	$^\circ C/W$

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	60	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	13.5	17	$m\Omega$
		$V_{GS}=4.5V$, $I_D=15A$	---	18	23	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.2	1.8	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=48V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	1.2	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=30V$, $V_{GS}=10V$, $I_D=18A$	---	57	---	nC
Q_{gs}	Gate-Source Charge		---	8.7	---	
Q_{gd}	Gate-Drain Charge		---	14	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V$, $V_{GS}=10V$, $R_G=3.3\Omega$, $I_D=20A$	---	16.2	---	ns
T_r	Rise Time		---	41.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	56.4	---	
T_f	Fall Time		---	16.2	---	
C_{iss}	Input Capacitance	$V_{DS}=30V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	1260	---	pF
C_{oss}	Output Capacitance		---	139	---	
C_{rss}	Reverse Transfer Capacitance		---	87	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	50	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=20A$, $dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	72	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=50V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=40A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

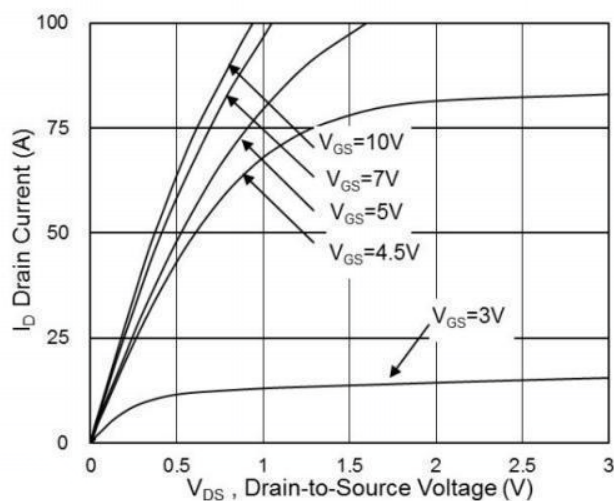


Fig.1 Typical Output Characteristics

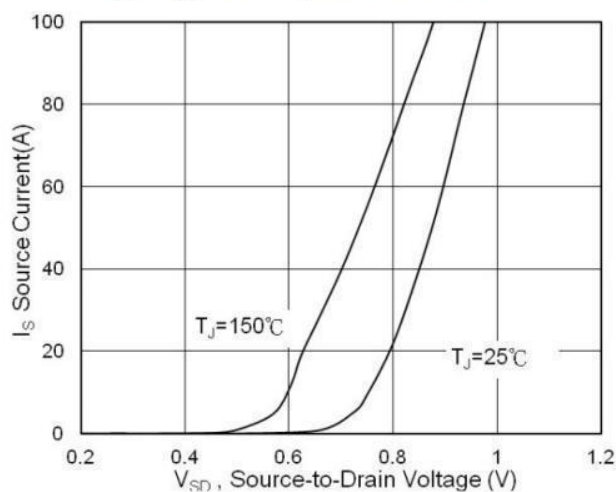


Fig.3 Forward Characteristics of Reverse

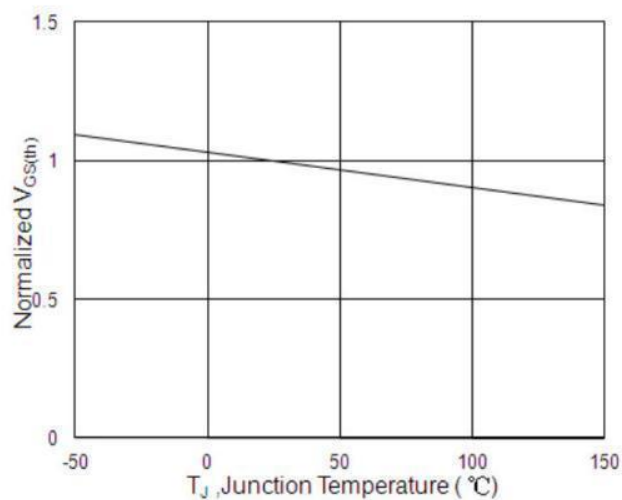


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

60V N-Channel Enhancement Mode MOSFET

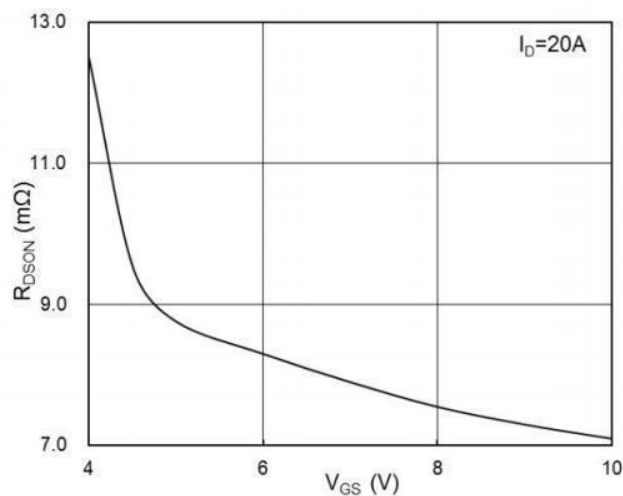


Fig.2 On-Resistance v.s Gate-Source

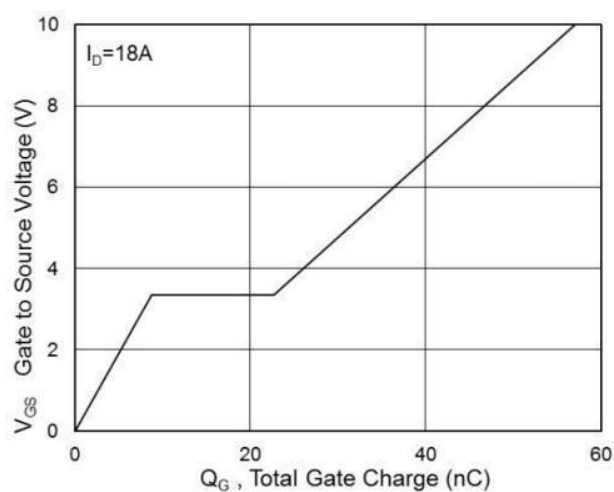


Fig.4 Gate-Charge Characteristics

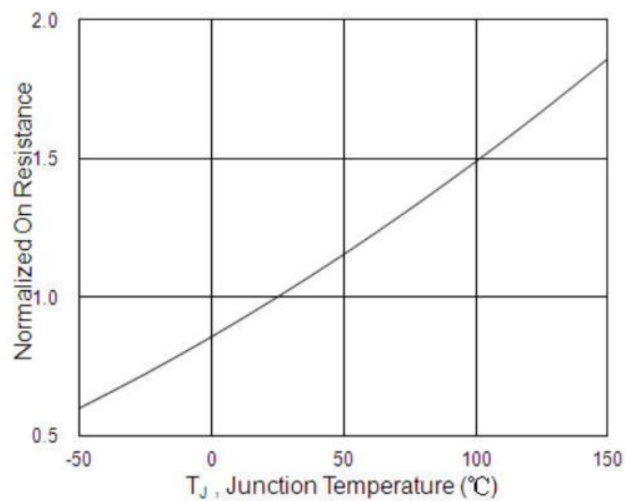


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

60V N-Channel Enhancement Mode MOSFET

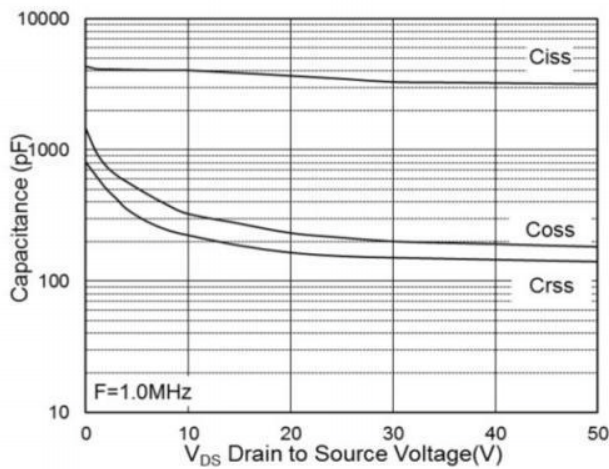


Fig.7 Capacitance

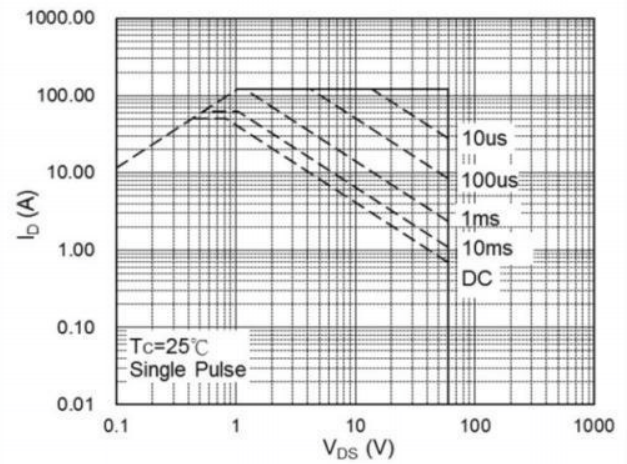


Fig.8 Safe Operating Area

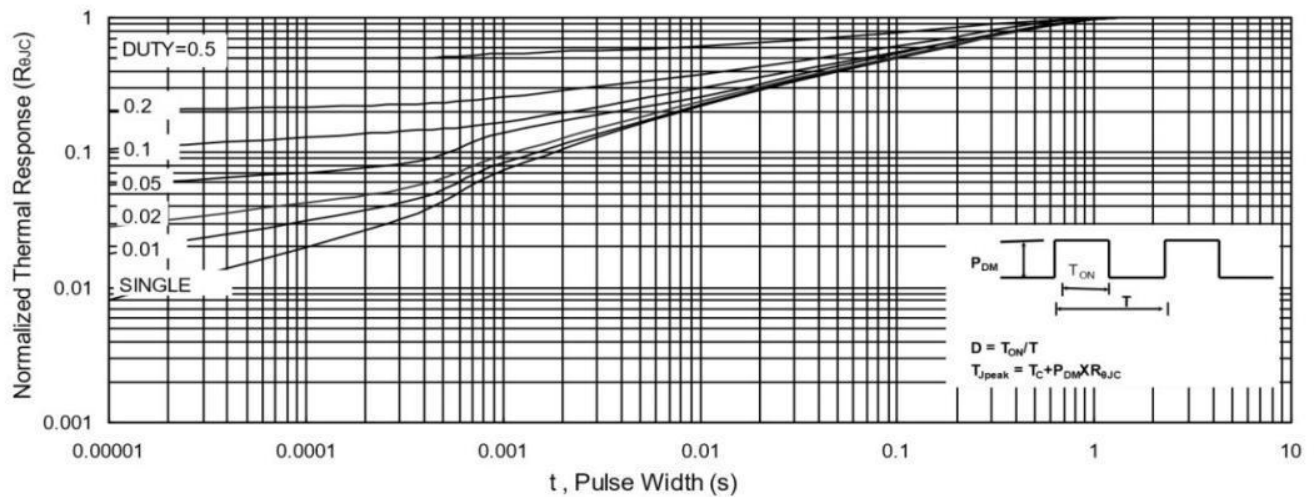


Fig.9 Normalized Maximum Transient Thermal Impedance

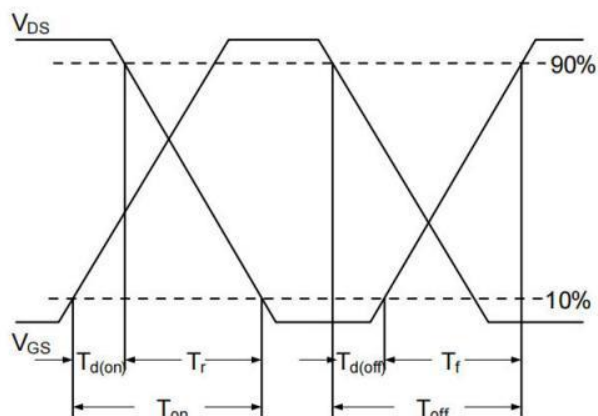


Fig.10 Switching Time Waveform

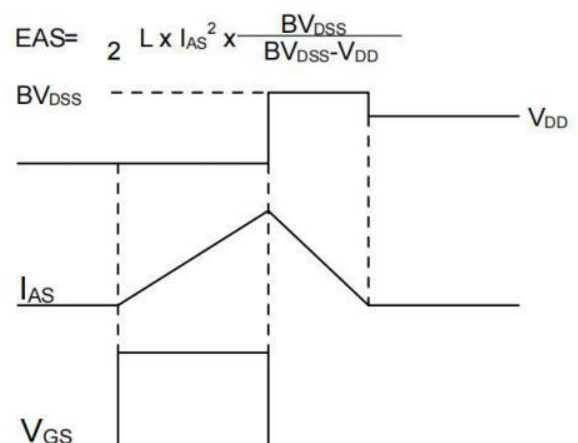
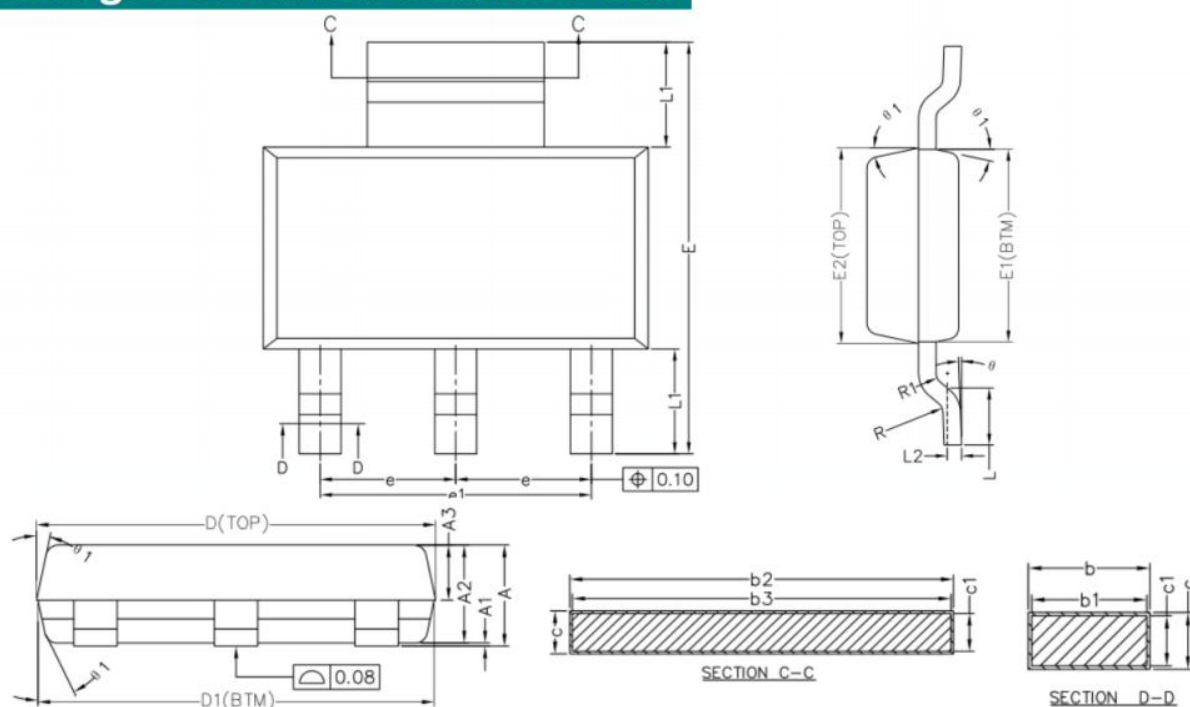


Fig.11 Unclamped Inductive Switching Waveform

60V N-Channel Enhancement Mode MOSFET

Package Mechanical Data-SOT-223



Symbol	Min	Nom	Max
A	--	--	1.80
A1	0.02	--	0.10
A2	1.50	1.60	1.70
A3	0.80	0.90	1.00
b	0.67	--	0.80
b1	0.66	0.71	0.76
b2	2.96	--	3.09
b3	2.95	3.00	3.05
C	0.30	--	0.35
C1	0.29	0.30	0.31
D	6.48	6.53	6.58
D1	6.55	6.60	6.65
E	6.80	--	7.20
E1	3.40	3.50	3.60
E2	3.33	3.43	3.53
e	2.30BSC		
e1	4.60BSC		
L	0.80	1.00	1.20
L1	1.75REF		
L2	0.25BSC		
R	0.10	--	--
R1	0.10	--	--
θ	0°	--	8°
θ1	10°	12°	14°

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