

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRFB3307Z
▶ Overseas	Part Number	IRFB3307Z
▶ Equivalent	Part Number	IRFB3307Z

EV is the abbreviation of name EVVO

80V N-SGT Enhancement Mode MOSFET

Description

The IRFB3307Z use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching. This device is specially designed to get better ruggedness and suitable to use in

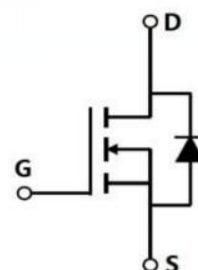
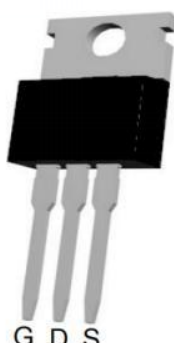
Application

Consumer electronic power supply Motor control
 Synchronous-rectification Isolated DC
 Synchronous-rectification applications

General Features

Low $R_{DS(on)}$ & FOM
 Extremely low switching loss
 Excellent stability and uniformity or Invertors

TO-263/TO-220-3L Pin Configuration



Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	80	V
Gate source voltage	VGS	± 20	V
Continuous drain current ¹⁾	ID	152	A
Pulsed drain current ²⁾	ID, pulse	390	A
Power dissipation ³⁾	P _D	192	W
Single pulsed avalanche energy ⁵⁾	EAS	400	mJ
Operation and storage temperature	T _{stg} , T _j	-55 to 150	°C
Thermal resistance, junction-case	R θ JC	0.65	°C/W
Thermal resistance, junction-ambient ⁴⁾	R θ JA	62.5	°C/W

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Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	80			V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	2.0		4.0	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		3.5	4.5	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		8681		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		6484		pF	
Reverse transfer capacitance	C_{rss}		8.55		pF	
Turn-on delay time	$t_{d(on)}$		28.2		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2.2\text{ }\Omega$, $I_D=22\text{ A}$
Rise time	t_r		7.5		ns	
Turn-off delay time	$t_{d(off)}$		81.9		ns	
Fall time	t_f		20.1		ns	
Total gate charge	Q_g		101.6		nC	$I_D=22\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$
Gate-source charge	Q_{gs}		20.6		nC	
Gate-drain charge	Q_{gd}		28.7		nC	
Gate plateau voltage	$V_{plateau}$		4.2		V	
Diode forward current	I_S			152	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			390		
Diode forward voltage	V_{SD}			1.3	V	$I_S=20\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		82.1		ns	$I_S=10\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		248.4		nC	
Peak reverse recovery current	I_{rrm}		4.9		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25^{\circ}\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, $L=0.5\text{ mH}$, starting $T_J=25^{\circ}\text{C}$.

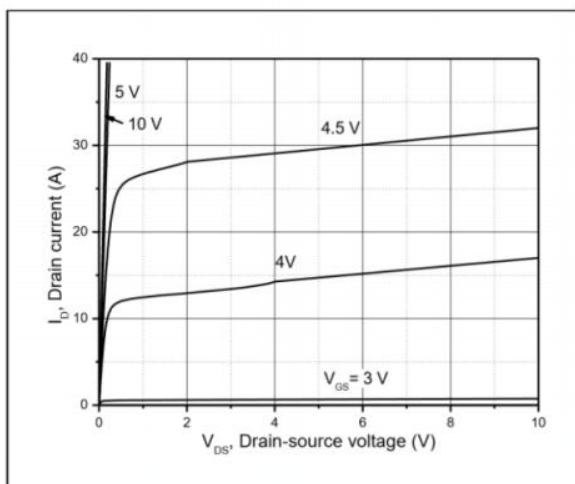
80V N-SGT Enhancement Mode MOSFET
Electrical Characteristics Diagrams


Figure 1, Typ. output characteristics

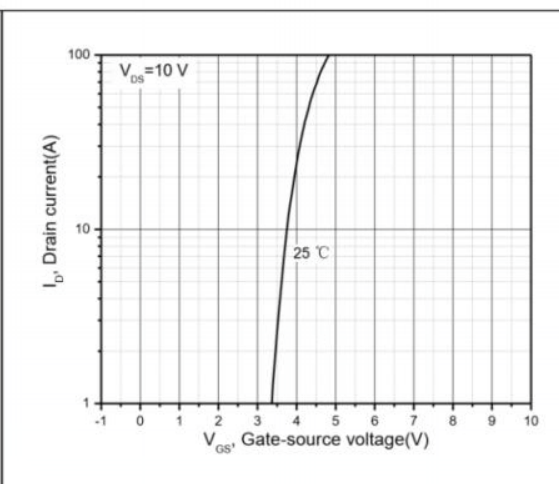


Figure 2, Typ. transfer characteristics

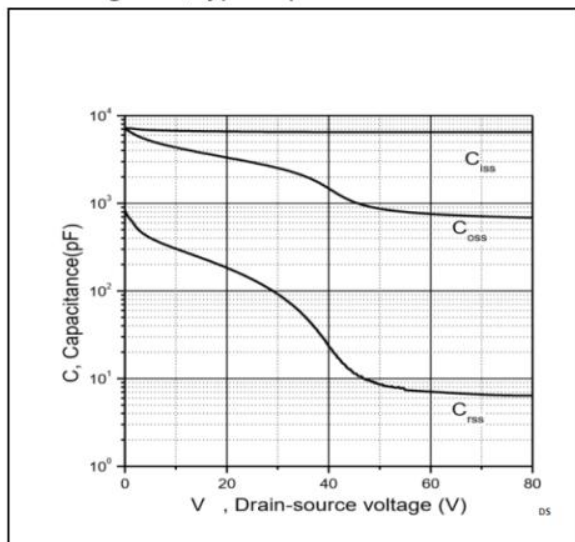


Figure 3, Typ. capacitances

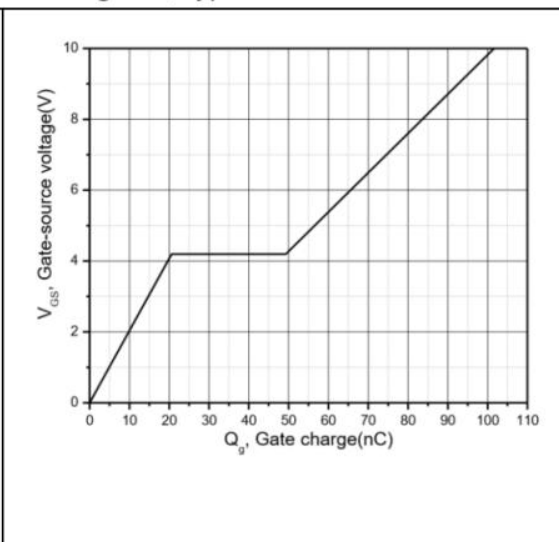


Figure 4, Typ. gate charge

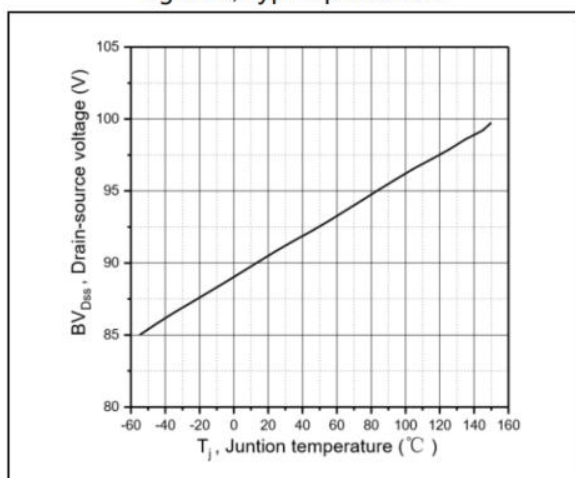


Figure 5, Drain-source breakdown voltage

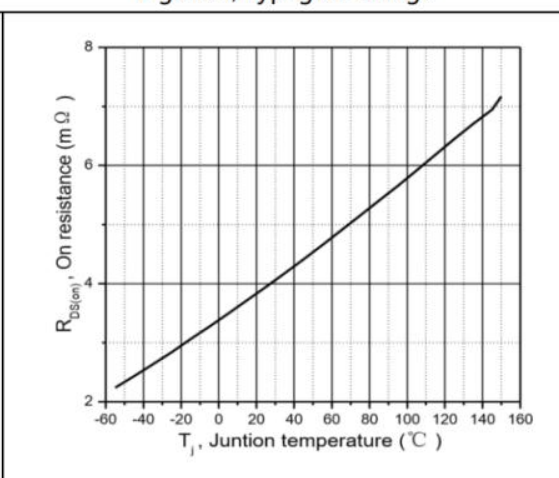


Figure 6, Drain-source on-state resistance

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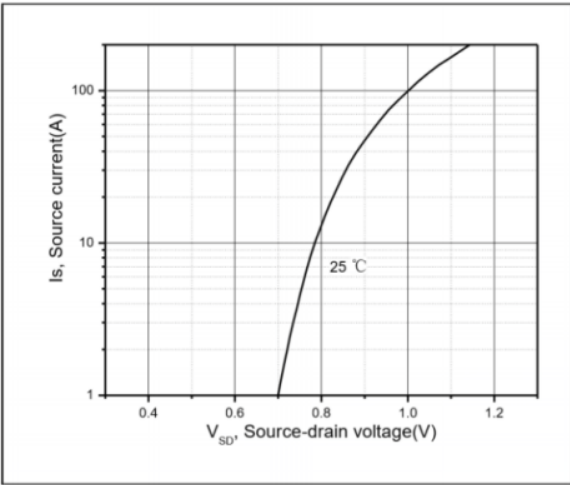


Figure 7, Forward characteristic of body diode

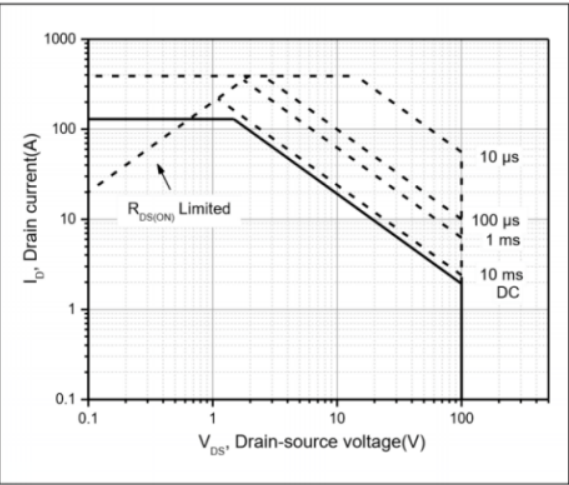


Figure 8, Safe operation area $T_C=25\text{ °C}$

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Test circuits and waveforms

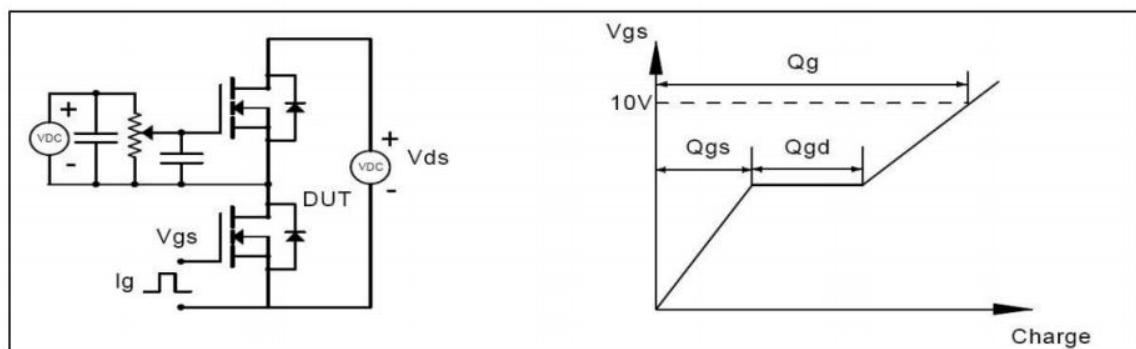


Figure 1, Gate charge test circuit & waveform

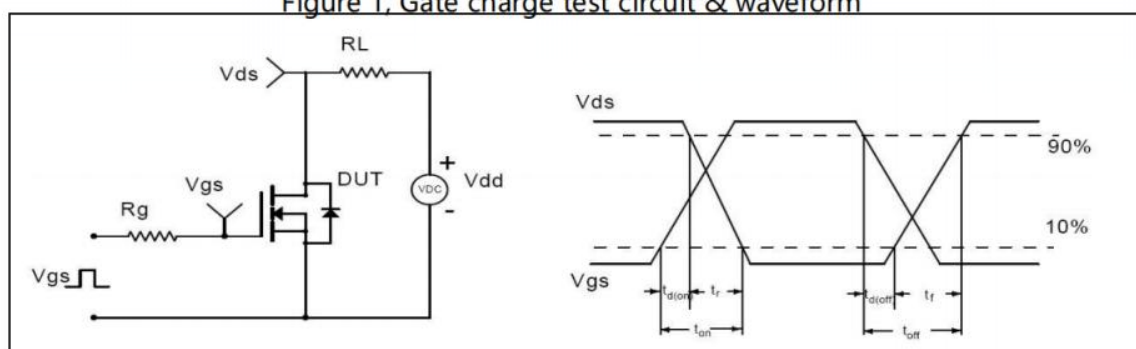


Figure 2, Switching time test circuit & waveforms

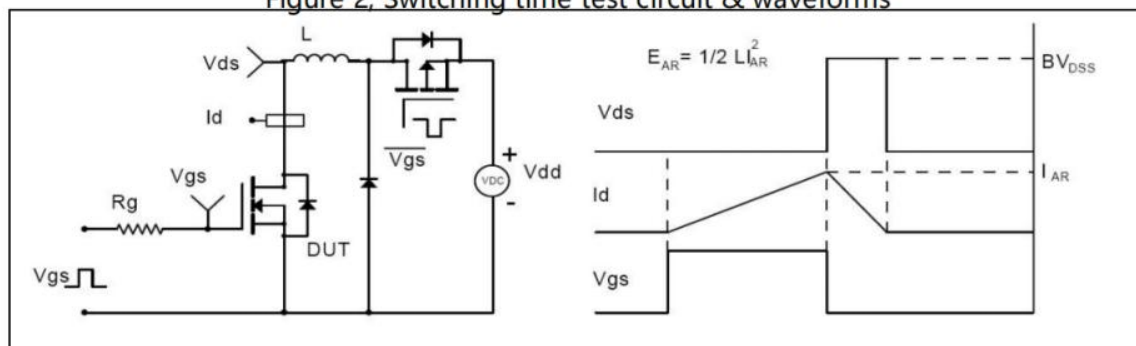


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

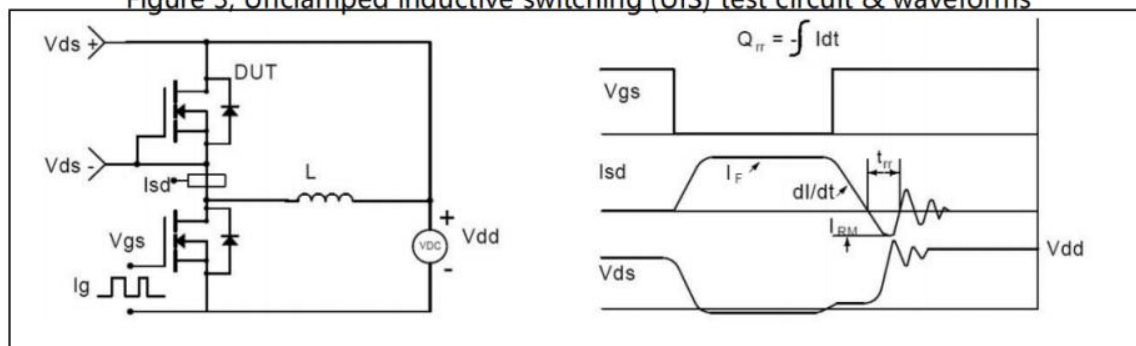
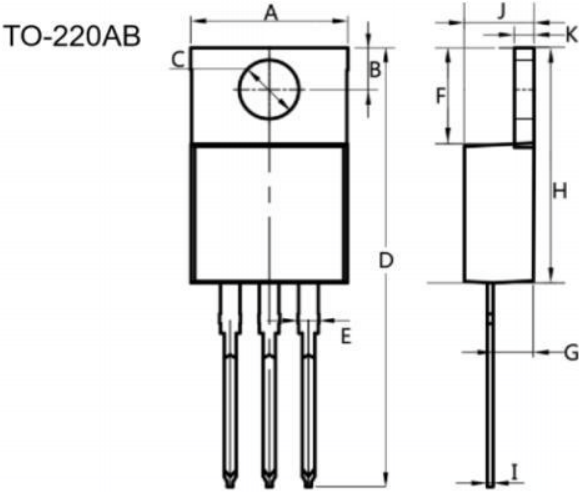


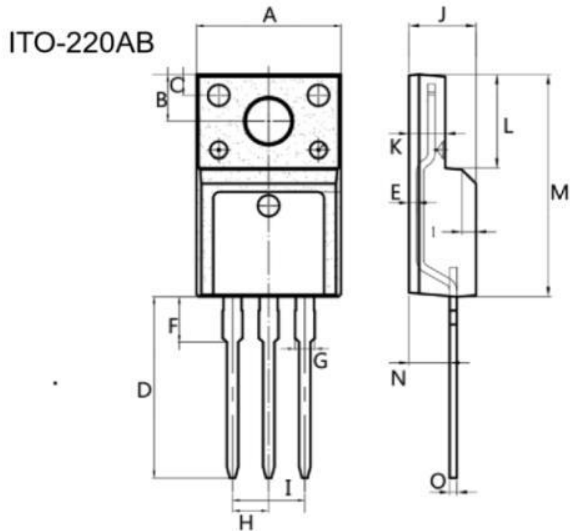
Figure 4, Diode reverse recovery test circuit & waveforms

80V N-SGT Enhancement Mode MOSFET



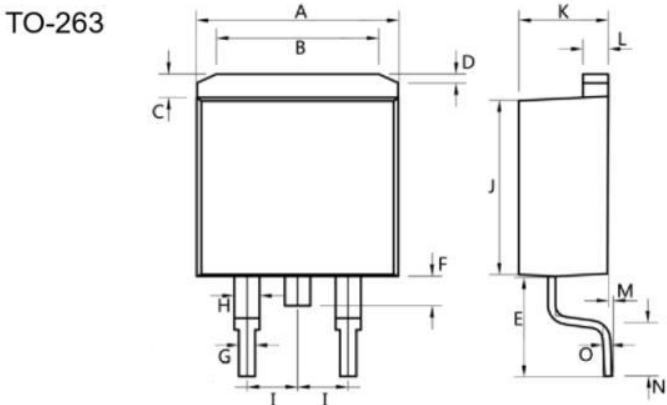
Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4

All Dimensions in millimeter



Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2.7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60

All Dimensions in millimeter



Dim.	Min.	Max.
A	10.0	10.5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45

All Dimensions in millimeter

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