

EVVOSEMI[®]

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TVS



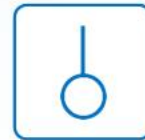
MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRLML6402
▶ Overseas	Part Number	IRLML6402
▶ Equivalent	Part Number	IRLML6402

EV is the abbreviation of name EVVO

-20V P-Channel Enhancement Mode MOSFET

Description

The IRLML6402 uses advanced trench It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

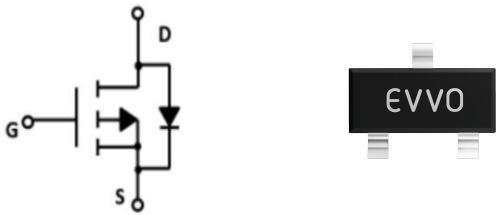
Application

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature

General Features

- $V_{DS} = -20V, I_D = -4.2A$
- $R_{DS(ON)} = 33m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} = 45m\Omega @ V_{GS}=2.5V$

SOT-23 Pin Configuration



Absolute max Rating: @T_A=25°C unless otherwise specified

Symbol	Parameter	Max.	Units
I _D @ TC = 25°C	Continuous Drain Current, V _{GS} @ 10V	-4.2①	A
I _D @ TC = 70°C	Continuous Drain Current, V _{GS} @ 10V	-2.4 ①	
I _{DM}	Pulsed Drain Current ②	-30	
P _D @TC = 25°C	Power Dissipation ③	1.4	W
V _{DS}	Drain-Source Voltage	-20	V
V _{GS}	Gate-to-Source Voltage	± 8	V
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
R _{θJA}	Junction-to-ambient (t ≤ 10s) ④	90	°C /W

-20V P-Channel Enhancement Mode MOSFET
Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-to-Source breakdown voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20	—	—	V
R _{DS(on)}	Static Drain-to-Source on-resistance	$V_{GS} = -4.5V, I_D = -4A$	—	33	35	mΩ
		$V_{GS} = -2.5V, I_D = -4A$	—	45	54	
		$V_{GS} = -1.8V, I_D = -2A$	—	60	70	
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.3	—	-1.0	V
		$T_J = 125^\circ\text{C}$	—	-0.44	—	
IDSS	Drain-to-Source leakage current	$V_{DS} = -16V, V_{GS} = 0V$	—	—	-1	μA
		$T_J = 125^\circ\text{C}$	—	—	-50	
IGSS	Gate-to-Source forward leakage	$V_{GS} = 8V$	—	—	10	μA
		$V_{GS} = -8V$	—	—	-10	
Q _g	Total gate charge	$I_D = -4A,$ $V_{DS} = -10V,$ $V_{GS} = -4.5V$	—	10	—	nC
Q _{gs}	Gate-to-Source charge		—	0.77	—	
Q _{gd}	Gate-to-Drain("Miller") charge		—	3.5	—	
t _{d(on)}	Turn-on delay time	$V_{GS} = -4.5V, V_{DS} = -10V,$ $R_{GEN} = 3\Omega,$	—	10	—	ns
t _r	Rise time		—	8.6	—	
t _{d(off)}	Turn-Off delay time		—	29	—	
t _f	Fall time		—	13	—	
C _{iss}	Input capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 1\text{MHz}$	—	886.6	—	pF
C _{oss}	Output capacitance		—	140.6	—	
C _{rss}	Reverse transfer capacitance		—	129.2	—	

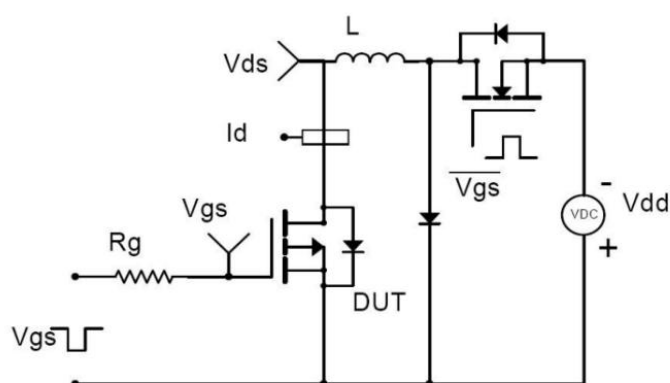
Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of R_{θJA} is measured with the device mounted on 1 in 2 FR 4 board with 2oz. Copper, in a still air environment with T_A = 25°C

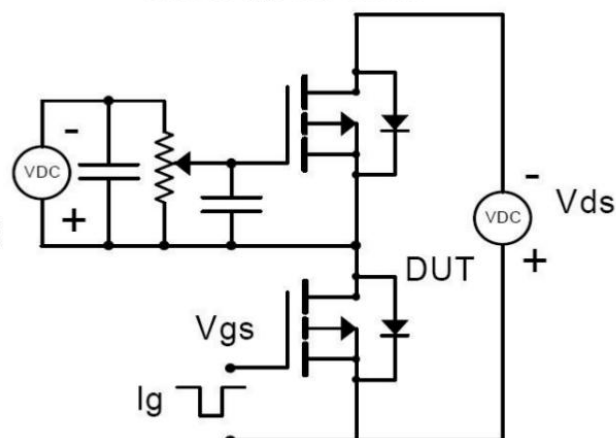
-20V P-Channel Enhancement Mode MOSFET

Test circuits and Waveforms

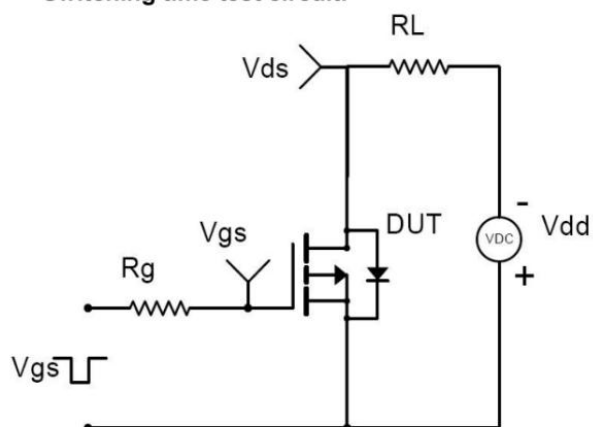
EAS test circuit:



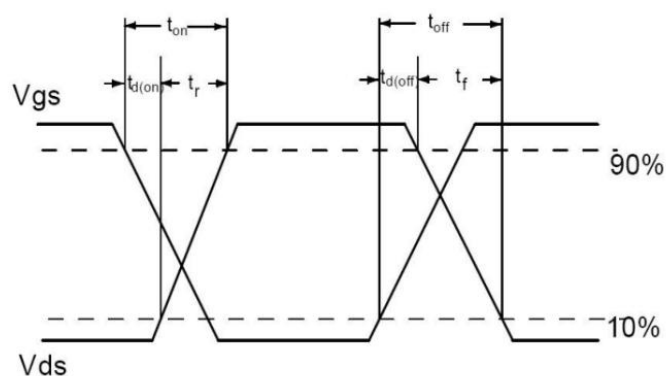
Gate charge test circuit:



Switching time test circuit:



Switch Waveforms:



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Typical electrical and thermal characteristics

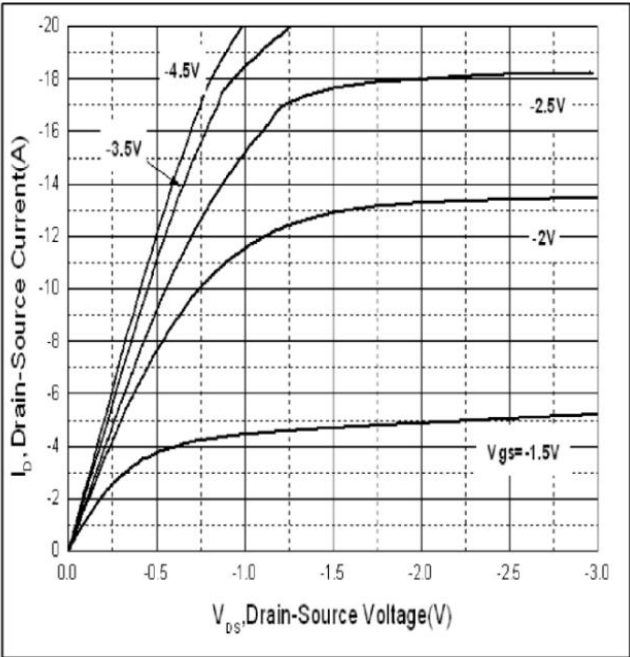


Figure 1: Typical Output Characteristics

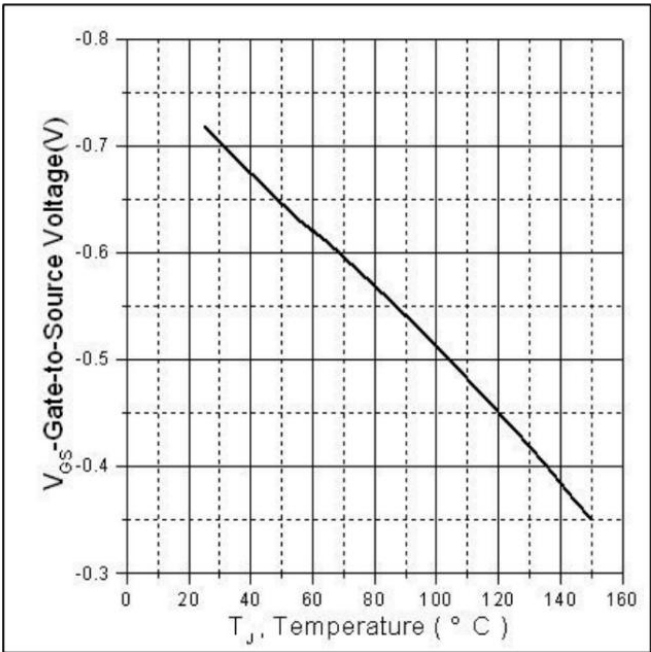


Figure 2: Gate to source cut-off voltage

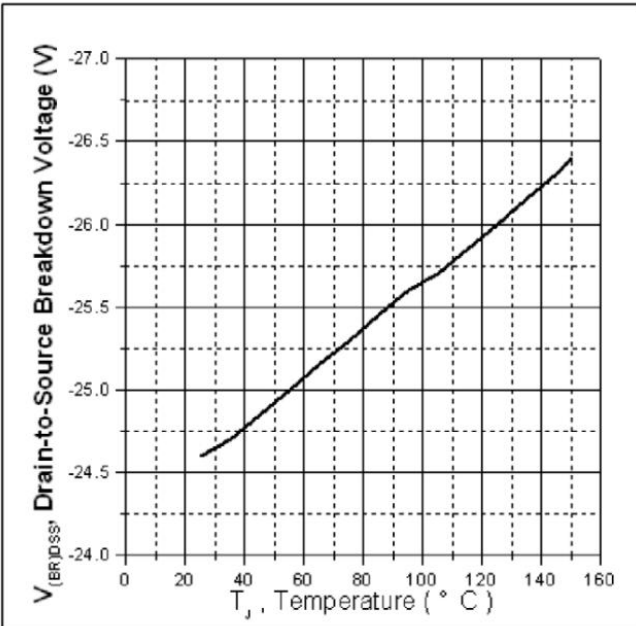


Figure 3: Drain-to-Source Breakdown Voltage Vs.
Case Temperature

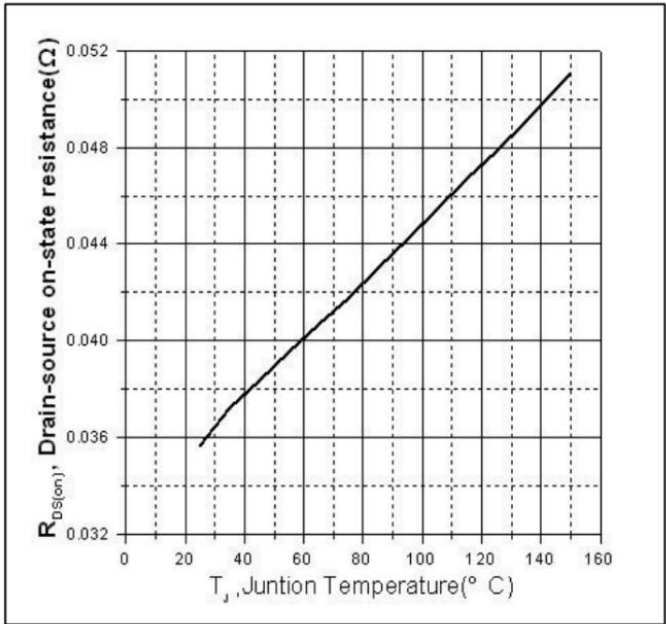


Figure 4: Normalized On-Resistance Vs. Case
Temperature

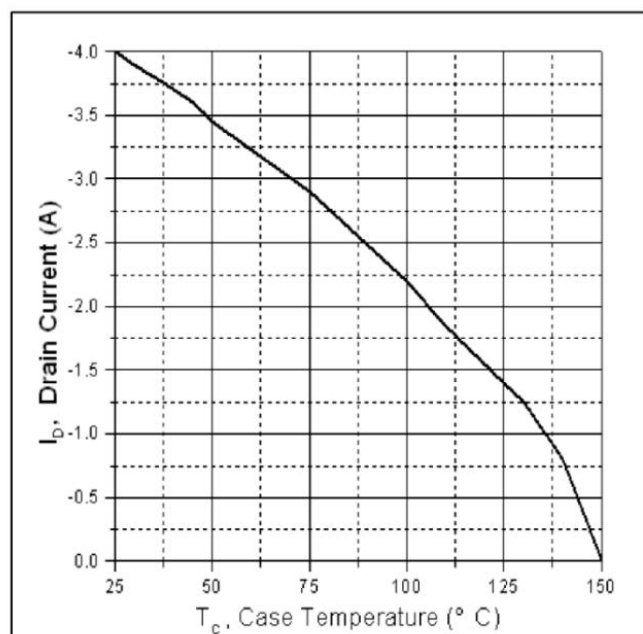
-20V P-Channel Enhancement Mode MOSFET
Typical electrical and thermal characteristics


Figure 5. Maximum Drain Current Vs. Case Temperature

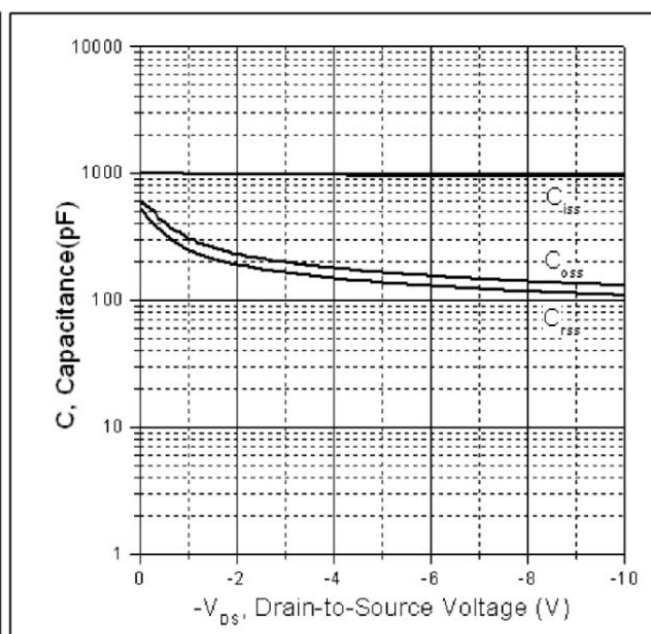


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

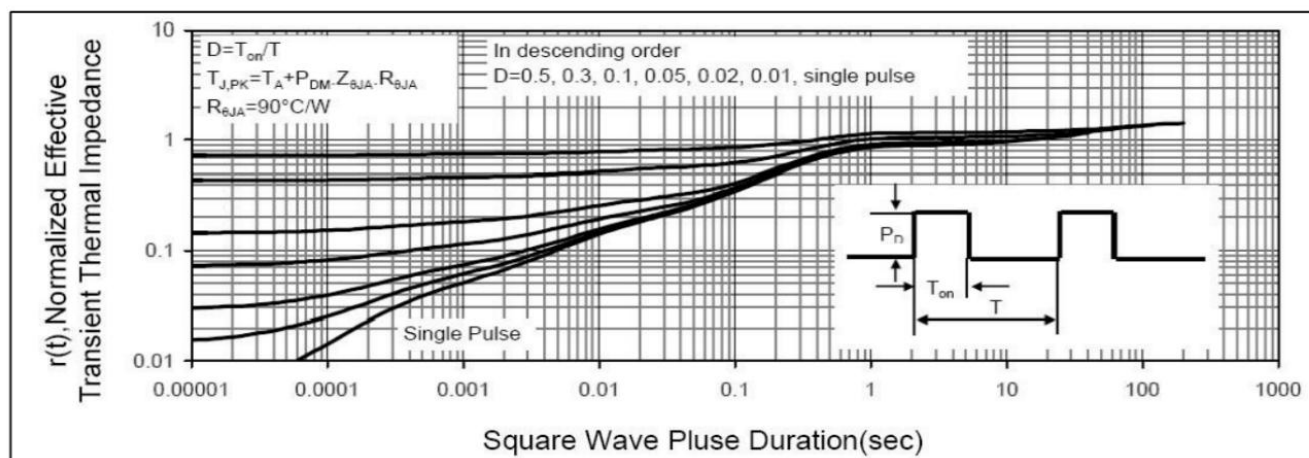
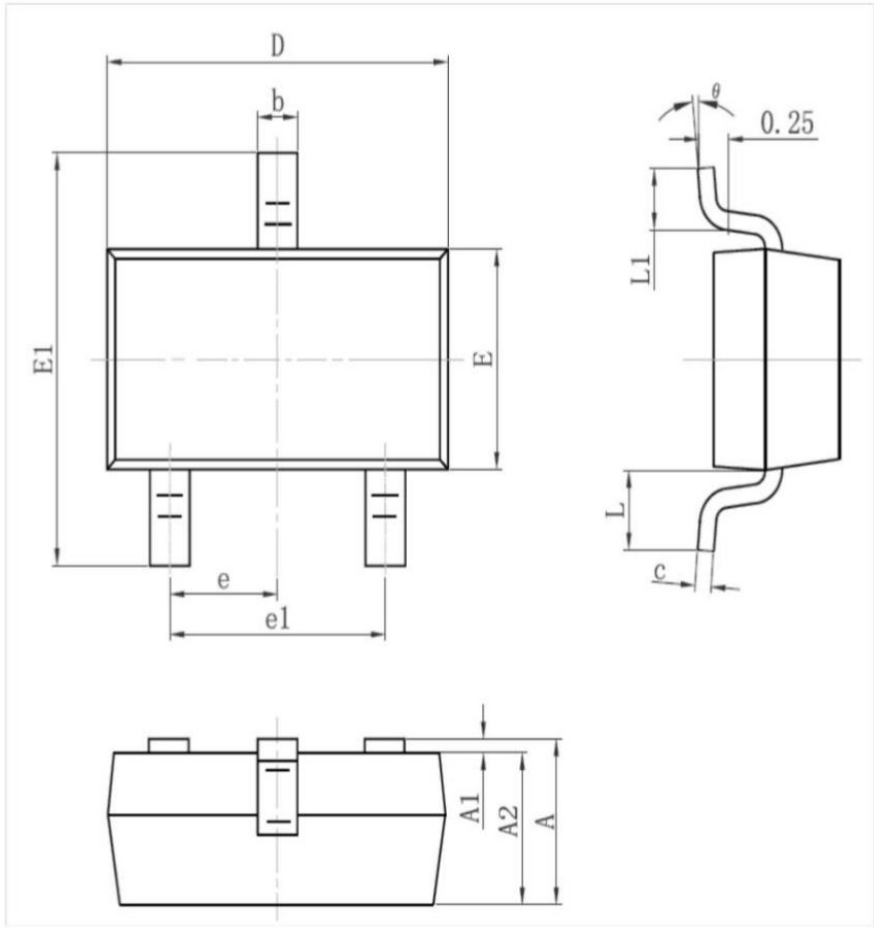


Figure7. Maximum Effective Transient Thermal Impedance Junction-to-Case

-20V P-Channel Enhancement Mode MOSFET

Mechanical Data

SOT-23 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.95TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.55REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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