



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic Part Number	IRF7343
▶ Overseas Part Number	IRF7343
▶ Equivalent Part Number	IRF7343



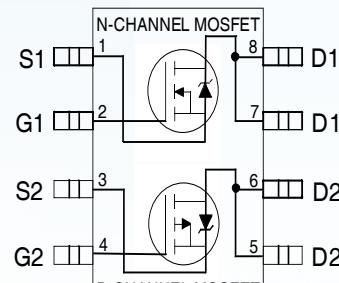
Dual N+ P Channel MOSFET
Features

N-Ch:

- $V_{DS(V)} = 55V$
- $R_{DS(ON)} < 50m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 65 m\Omega$ ($V_{GS} = 4.5V$)

P-Ch:

- $V_{DS(V)} = -55V$
- $R_{DS(ON)} < 90m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 100m\Omega$ ($V_{GS} = 4.5V$)
- Generation V Technology
- Ultra Low On-Resistance
- Surface Mount
- Fully Avalanche Rated
- Lead-Free



Top View

Description

The SOP-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. with these improvements. mutipe devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	55	-55	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.7	-3.4	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.8	-2.7	
I_{DM}	Pulsed Drain Current ①	38	-27	
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation ⑤	2.0		W
$P_D @ T_A = 70^\circ C$	Maximum Power Dissipation ⑤	1.3		W
E_{AS}	Single Pulse Avalanche Energy ③	72	114	mJ
I_{AR}	Avalanche Current	4.7	-3.4	A
E_{AR}	Repetitive Avalanche Energy	0.20		mJ
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④		62.5	°C/W

Dual N+ P Channel MOSFET
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	N-Ch 55			V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
		P-Ch -55				$V_{GS} = 0V, I_D = -250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	N-Ch 0.059			V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch 0.054				Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(\text{ON})}$	Static Drain-to-Source On-Resistance	N-Ch 43	50		m Ω	$V_{GS} = 10V, I_D = 4.7\text{A}$ ④
			56	65		$V_{GS} = 4.5V, I_D = 3.8\text{A}$ ④
		P-Ch 70	90			$V_{GS} = -10V, I_D = -3.4\text{A}$ ④
			95	100		$V_{GS} = -4.5V, I_D = -2.7\text{A}$ ④
$V_{GS(\text{th})}$	Gate Threshold Voltage	N-Ch 1.0			V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
		P-Ch -1.0				$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
g_{fs}	Forward Transconductance	N-Ch 7.9			S	$V_{DS} = 10V, I_D = 4.5\text{A}$ ④
		P-Ch 3.3				$V_{DS} = -10V, I_D = -3.1\text{A}$ ④
I_{DSS}	Drain-to-Source Leakage Current	N-Ch 2.0			μA	$V_{DS} = 55V, V_{GS} = 0V$
		P-Ch -2.0				$V_{DS} = -55V, V_{GS} = 0V$
		N-Ch 25				$V_{DS} = 55V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
		P-Ch -25				$V_{DS} = -55V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P ±100			nA	$V_{GS} = \pm 20V$
	Total Gate Charge	N-Ch 24	36			N-Channel $I_D = 4.5\text{A}, V_{DS} = 44V, V_{GS} = 10V$ ④
Q_{gs}	Gate-to-Source Charge	P-Ch 26	38		nC	P-Channel $I_D = -3.1\text{A}, V_{DS} = -44V, V_{GS} = -10V$
	Gate-to-Drain ("Miller") Charge	N-Ch 2.3	3.4			
Q_{gd}		P-Ch 3.0	4.5			
		N-Ch 7.0	10			
$t_{d(on)}$	Turn-On Delay Time	P-Ch 8.4	13		ns	
		N-Ch 13	20			N-Channel $V_{DD} = 28V, I_D = 1.0\text{A}, R_G = 6.0\Omega, R_D = 16\Omega$ ④
t_r	Rise Time	P-Ch 10	15			P-Channel $V_{DD} = -28V, I_D = -1.0\text{A}, R_G = 6.0\Omega, R_D = 16\Omega$
		N-Ch 10	15			
$t_{d(off)}$	Turn-Off Delay Time	N-Ch 32	48			
		P-Ch 43	64			
t_f	Fall Time	N-Ch 13	20			
		P-Ch 22	32			
C_{iss}	Input Capacitance	N-Ch 740			pF	N-Channel $V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$
		P-Ch 690				P-Channel $V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	N-Ch 190				
		P-Ch 210				
C_{rss}	Reverse Transfer Capacitance	N-Ch 71				
		P-Ch 86				

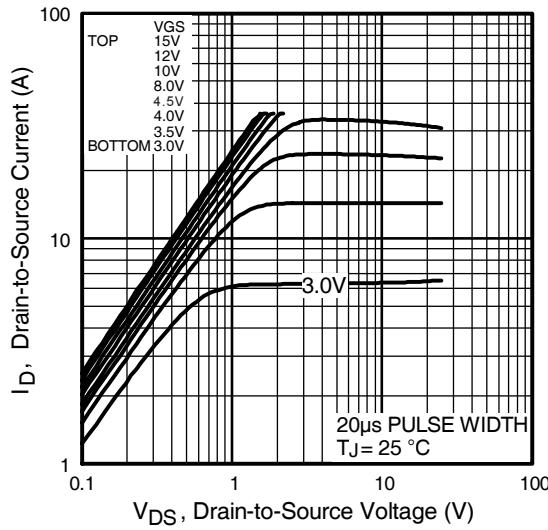
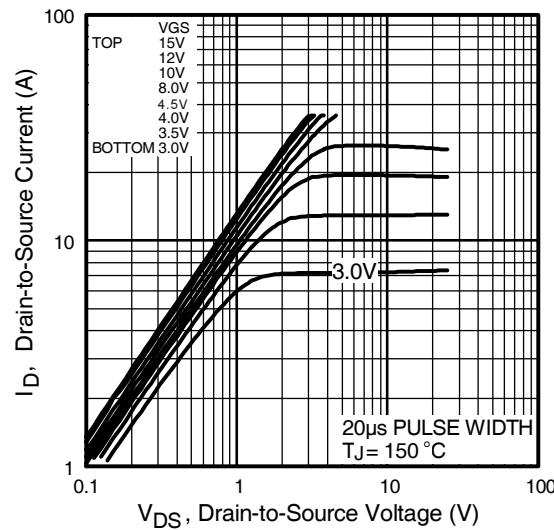
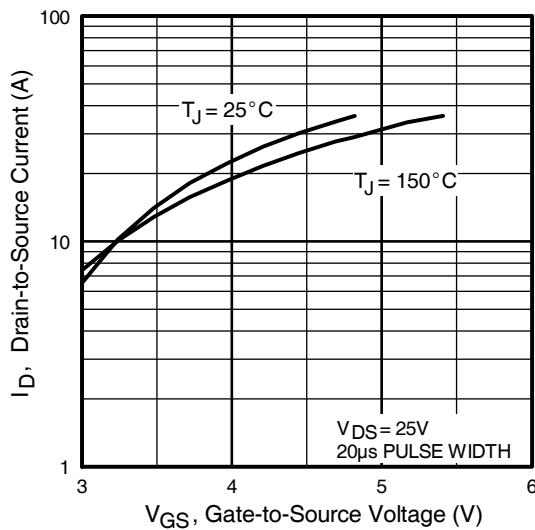
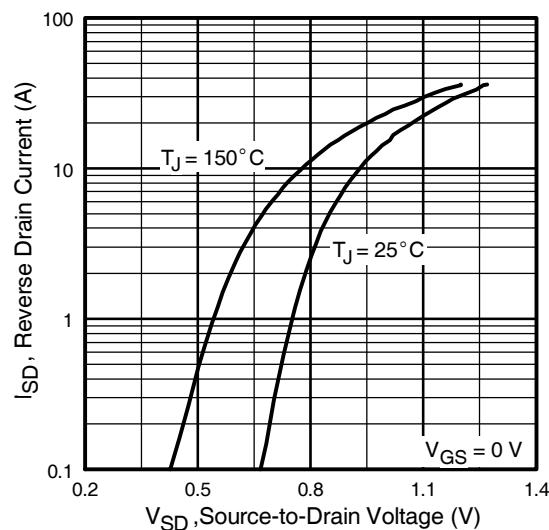
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch		2.0	A	
		P-Ch		-2.0		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch		38		
		P-Ch		-27		
V_{SD}	Diode Forward Voltage	N-Ch	0.70	1.2	V	$T_J = 25^\circ\text{C}, I_S = 2.0\text{A}, V_{GS} = 0V$ ③
		P-Ch	-0.80	-1.2		$T_J = 25^\circ\text{C}, I_S = -2.0\text{A}, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	60	90	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 2.0\text{A}, di/dt = 100\text{A}/\mu\text{s}$
		P-Ch	54	80		P-Channel $T_J = 25^\circ\text{C}, I_F = -2.0\text{A}, di/dt = 100\text{A}/\mu\text{s}$ ④
Q_{rr}	Reverse Recovery Charge	N-Ch	120	170	nC	
		P-Ch	85	130		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 22)
- ② N-Channel $I_{SD} \leq 4.7\text{A}, di/dt \leq 220\text{A}/\mu\text{s}, V_{DD} \leq V_{(\text{BR})\text{DSS}}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -3.4\text{A}, di/dt \leq -150\text{A}/\mu\text{s}, V_{DD} \leq V_{(\text{BR})\text{DSS}}, T_J \leq 150^\circ\text{C}$
- ③ N-Channel Starting $T_J = 25^\circ\text{C}, L = 6.5\text{mH} R_G = 25\Omega, I_{AS} = 4.7\text{A}$.
P-Channel Starting $T_J = 25^\circ\text{C}, L = 20\text{mH} R_G = 25\Omega, I_{AS} = -3.4\text{A}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

Dual N+ P Channel MOSFET

**Fig 1.** Typical Output Characteristics**Fig 2.** Typical Output Characteristics**Fig 3.** Typical Transfer Characteristics**Fig 4.** Typical Source-Drain Diode Forward Voltage

Dual N+ P Channel MOSFET

N-Channel

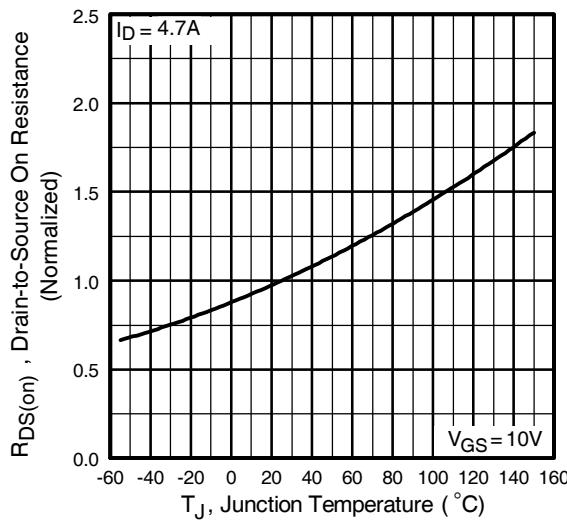


Fig 5. Normalized On-Resistance Vs. Temperature

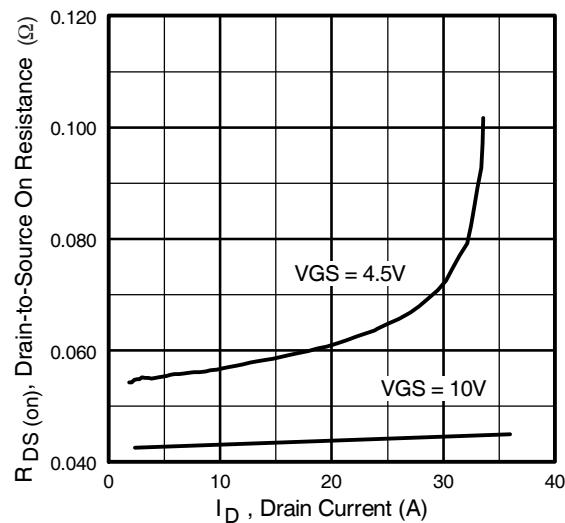


Fig 6. Typical On-Resistance Vs. Drain Current

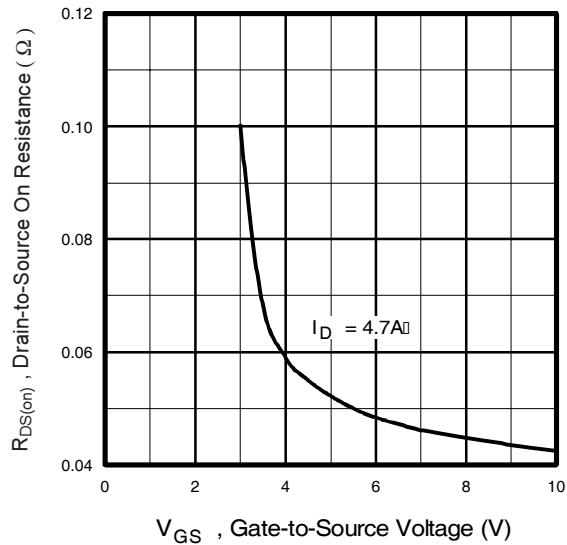


Fig 7. Typical On-Resistance Vs. Gate Voltage

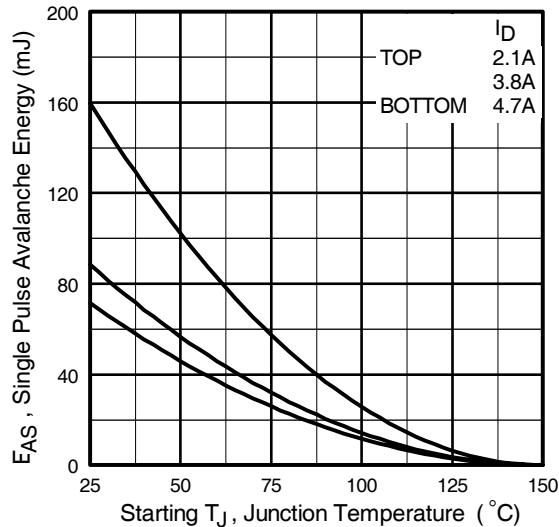


Fig 8. Maximum Avalanche Energy Vs. Drain Current

Dual N+ P Channel MOSFET

N-Channel

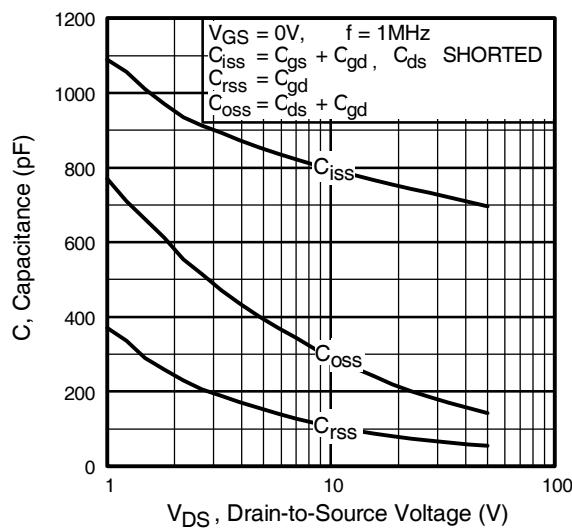


Fig 9. Typical Capacitance Vs.
Drain-to-Source Voltage

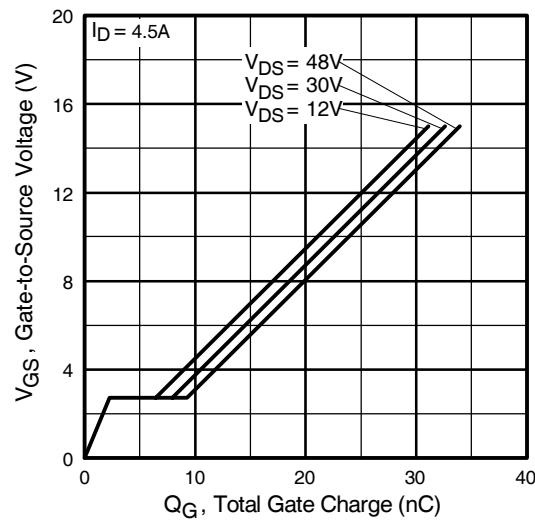


Fig 10. Typical Gate Charge Vs.
Gate-to-Source Voltage

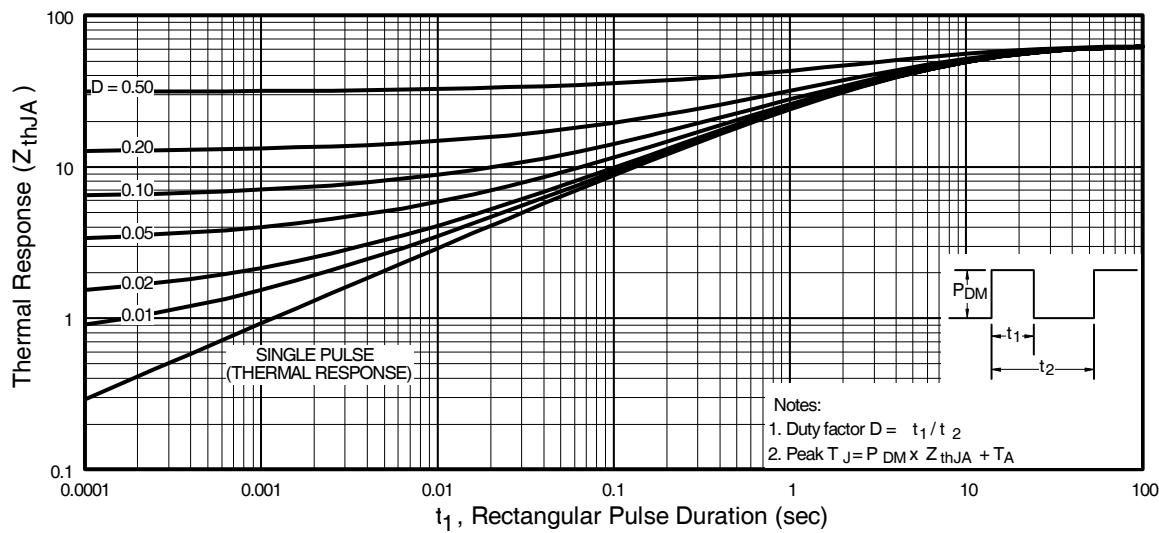
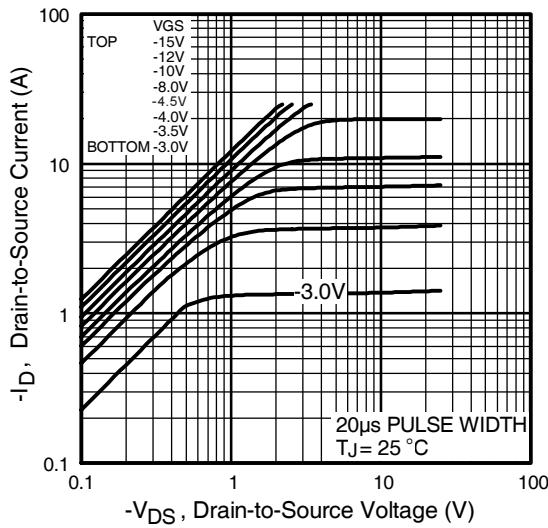
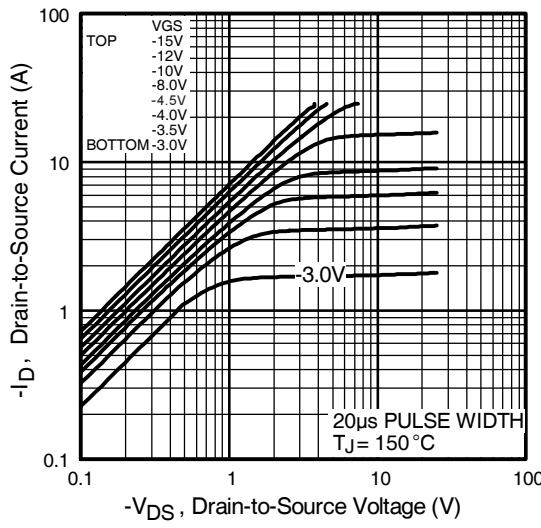
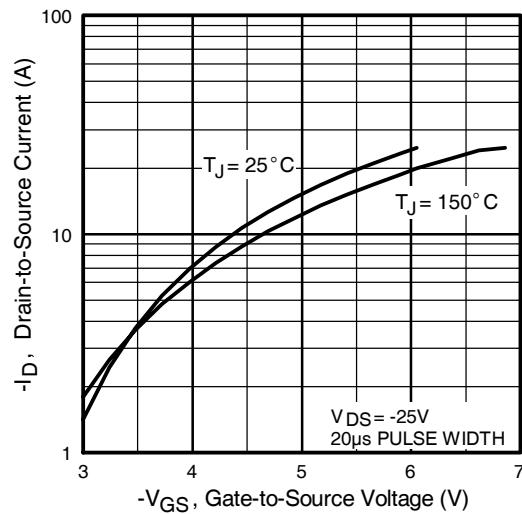
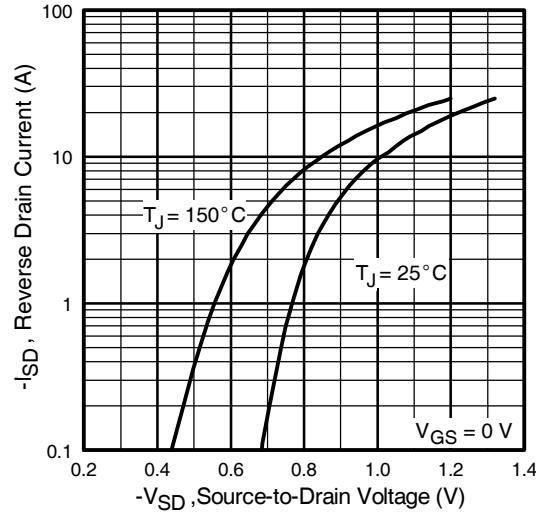


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Dual N+ P Channel MOSFET

P-Channel

**Fig 12.** Typical Output Characteristics**Fig 13.** Typical Output Characteristics**Fig 14.** Typical Transfer Characteristics**Fig 15.** Typical Source-Drain Diode Forward Voltage

Dual N+ P Channel MOSFET

P-Channel

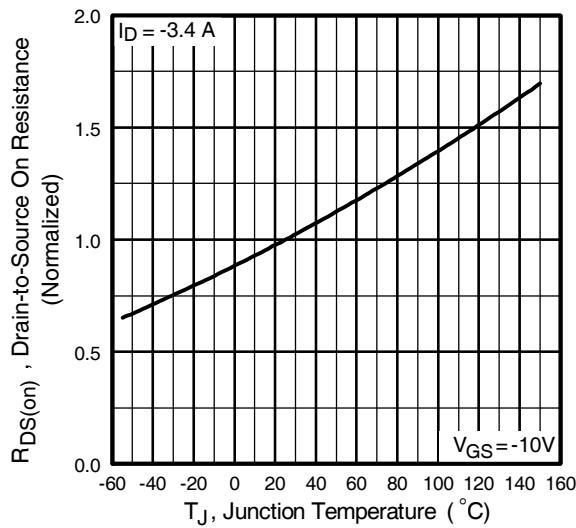


Fig 16. Normalized On-Resistance Vs. Temperature

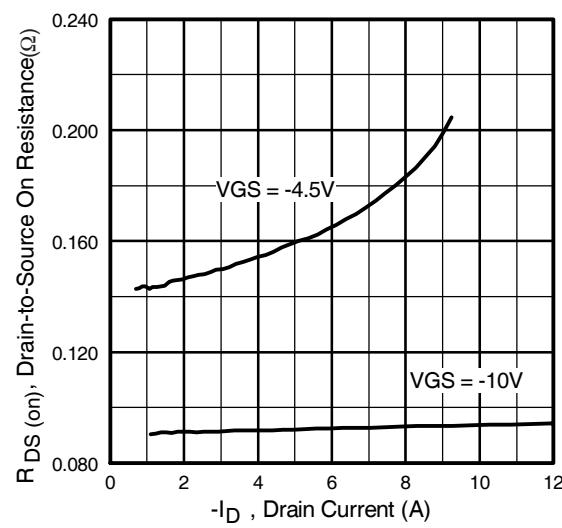


Fig 17. Typical On-Resistance Vs. Drain Current

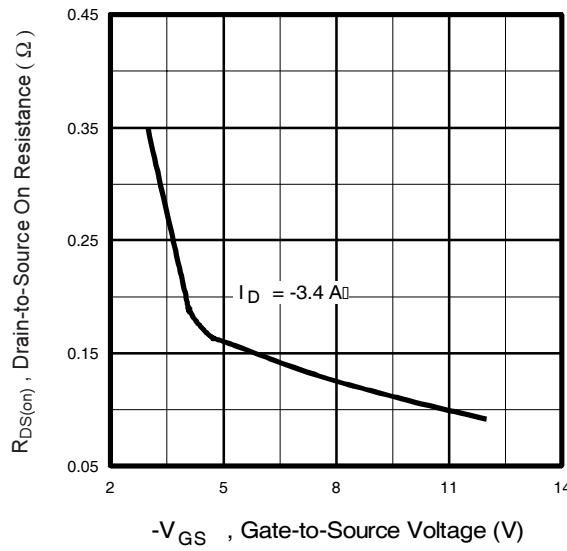


Fig 18. Typical On-Resistance Vs. Gate Voltage

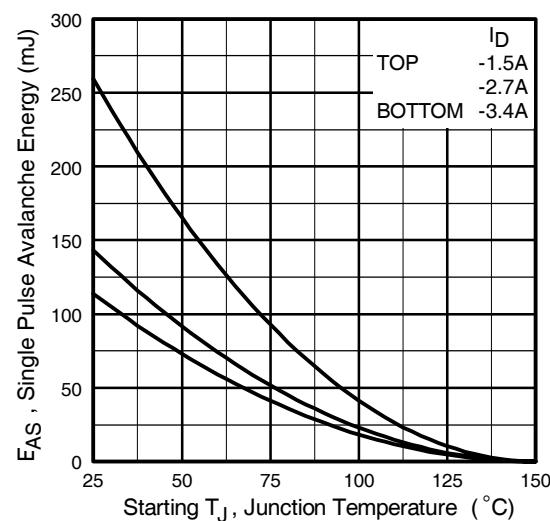


Fig 19. Maximum Avalanche Energy Vs. Drain Current

Dual N+ P Channel MOSFET

P-Channel

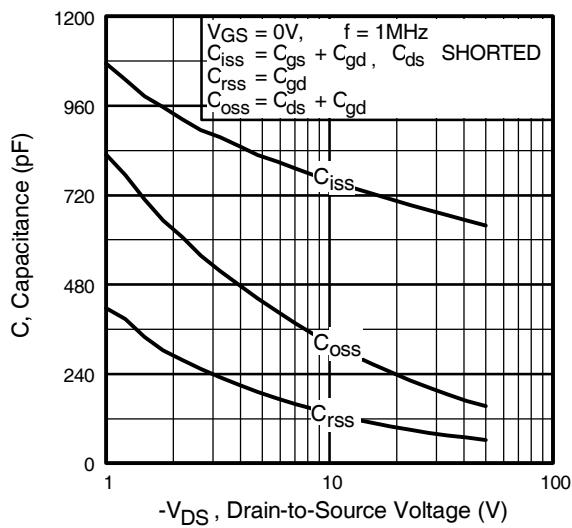


Fig 20. Typical Capacitance Vs.
Drain-to-Source Voltage

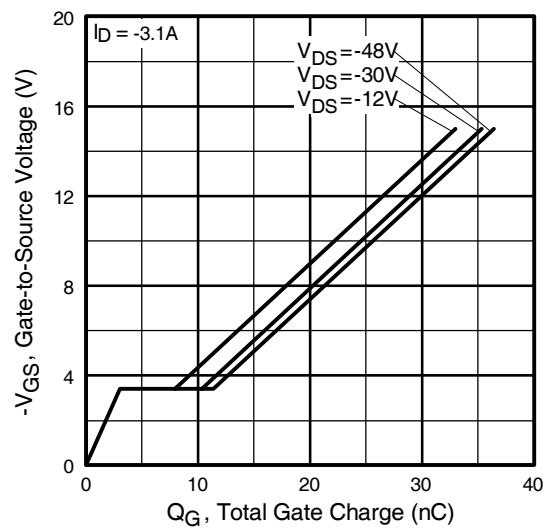


Fig 21. Typical Gate Charge Vs.
Gate-to-Source Voltage

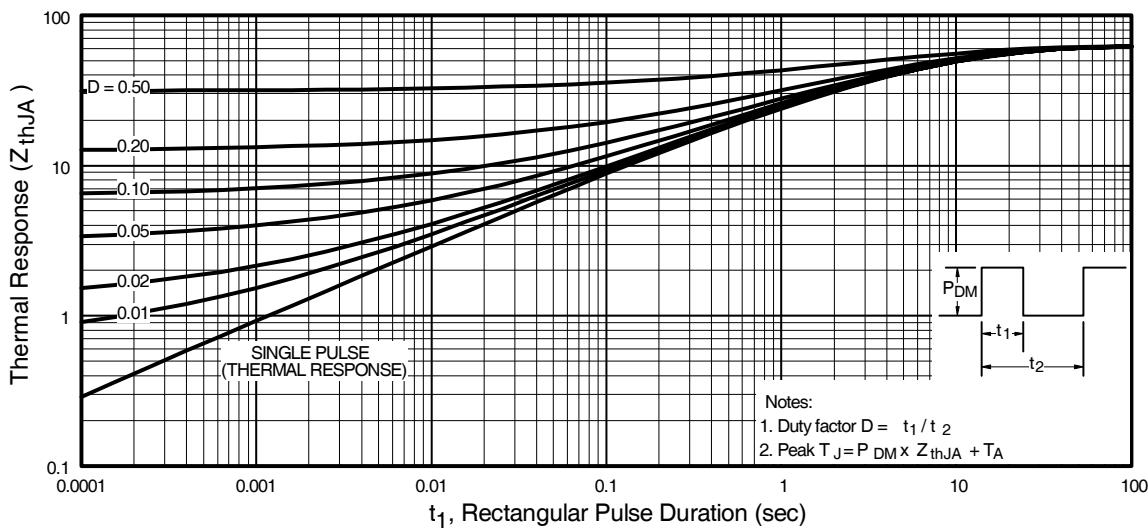
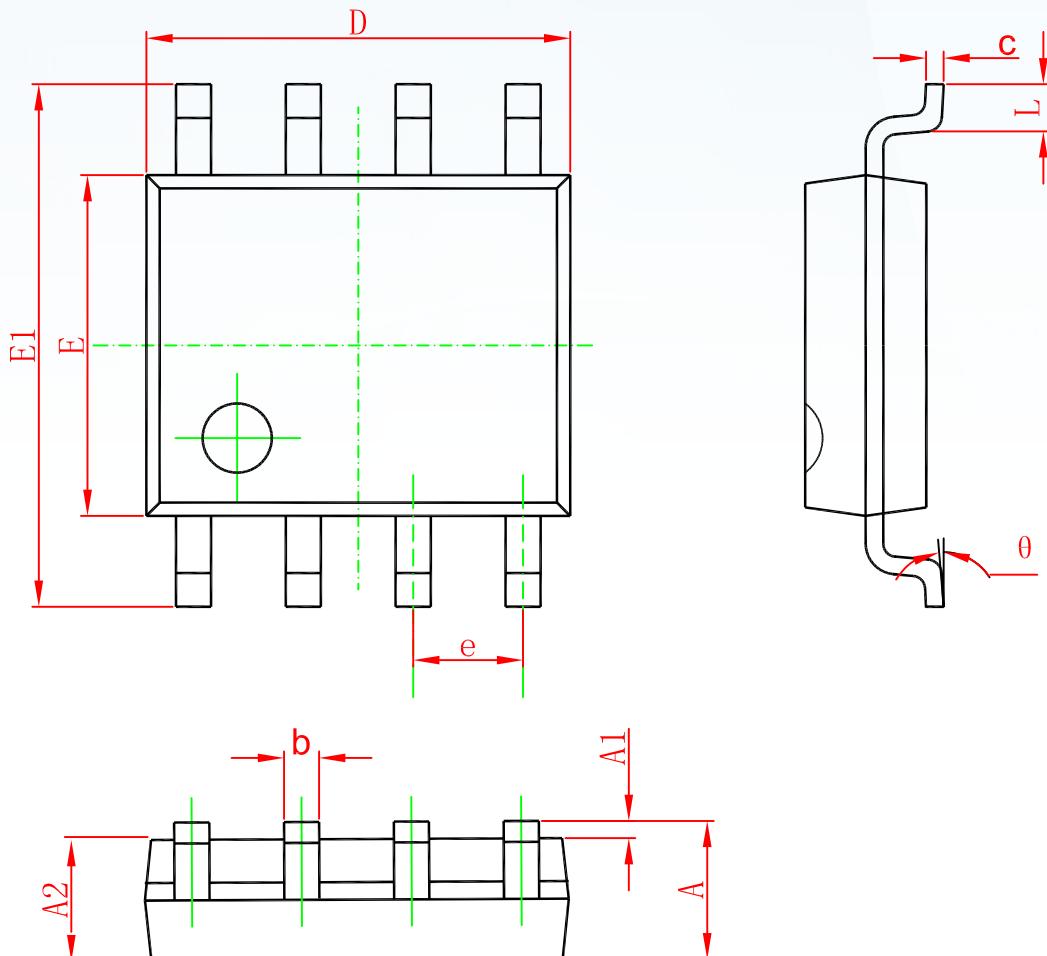


Fig 22. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Dual N+ P Channel MOSFET

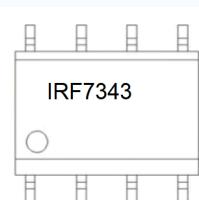
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Dual N+ P Channel MOSFET

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
IRF7343	SOP-8	3000	Tape and reel

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