

EVVOSEMI[®]

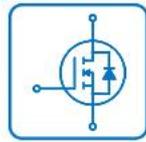
THINK CHANGE DO



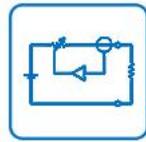
ESD



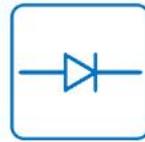
TVS



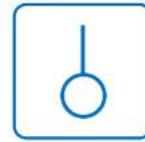
MOS



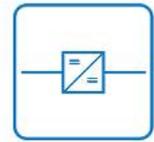
LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRF7105
▶ Overseas	Part Number	IRF7105
▶ Equivalent	Part Number	IRF7105

EV is the abbreviation of name EVVO

Dual N+ P Channel MOSFET

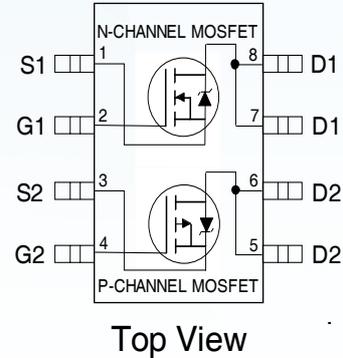
Features

N-Ch:

- $V_{DS} (V) = 25V$
- $R_{DS(ON)} < 100m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 160 m\Omega$ ($V_{GS} = 4.5V$)

P-Ch:

- $V_{DS} (V) = -25V$
- $R_{DS(ON)} < 250m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 400 m\Omega$ ($V_{GS} = 4.5V$)
- Advanced Process Technology Ultra
- Low On-Resistance
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free



Description

The SOP-8 has been modified through a customized eadframe "or enhanced therma characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave solderino techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.5	-2.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.8	-1.8	
I_{DM}	Pulsed Drain Current ①	14	-10	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	3.0	-3.0	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④			62.5	°C/W

Dual N+ P Channel MOSFET

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	N-Ch 25 P-Ch -25			V	V _{GS} = 0V, I _D = 250μA V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	N-Ch P-Ch	0.030 -0.015		V/°C	Reference to 25°C, I _D = 1mA Reference to 25°C, I _D = -1mA
R _{DS(ON)}	N-Ch P-Ch	83 140 160 300	100 160 250 400	mΩ	V _{GS} = 10V, I _D = 1.0A ③ V _{GS} = 4.5V, I _D = 0.50A ③ V _{GS} = -10V, I _D = -1.0A ③ V _{GS} = -4.5V, I _D = -0.50A ③
V _{GS(th)}	N-Ch P-Ch	1.0 -1.0	3.0 -3.0	V	V _{DS} = V _{GS} , I _D = 250μA V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	N-Ch P-Ch	4.3 3.1		S	V _{DS} = 15V, I _D = 3.5A ③ V _{DS} = -15V, I _D = -3.5A ③
I _{DSS}	N-Ch P-Ch N-Ch P-Ch		2.0 -2.0 25 -25	μA	V _{DS} = 20V, V _{GS} = 0V V _{DS} = -20V, V _{GS} = 0V V _{DS} = 20V, V _{GS} = 0V, T _J = 55°C V _{DS} = -20V, V _{GS} = 0V, T _J = 55°C
I _{GSS}	N-P		±100		V _{GS} = ± 20V
Q _g	N-Ch P-Ch	9.4 10	27 25	nC	N-Channel I _D = 2.3A, V _{DS} = 12.5V, V _{GS} = 10V ③
Q _{gs}	N-Ch P-Ch		1.7 1.9		P-Channel I _D = -2.3A, V _{DS} = -12.5V, V _{GS} = -10V
Q _{gd}	N-Ch P-Ch		3.1 2.8		
t _{d(on)}	N-Ch P-Ch	7.0 12	20 40	ns	N-Channel V _{DD} = 25V, I _D = 1.0A, R _G = 6.0Ω, R _D = 25Ω ③
t _r	N-Ch P-Ch	9.0 13	20 40		
t _{d(off)}	N-Ch P-Ch	45 45	90 90		P-Channel V _{DD} = -25V, I _D = -1.0A, R _G = 6.0Ω, R _D = 25Ω
t _f	N-Ch P-Ch	25 37	50 50		Between lead, 6mm (0.25in.) from package and center of die contact
L _S	N-P P-Ch	4.0 3.7	5.0	nH	
L _P	N-P	6.0			
C _{iss}	N-Ch P-Ch	330 290		pF	N-Channel V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz
C _{oss}	N-Ch P-Ch	250 210			P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
C _{rss}	N-Ch P-Ch	61 67			

Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	N-Ch P-Ch		2.0 -2.0	A	
I _{SM}	N-Ch P-Ch		14 -9.2		
V _{SD}	N-Ch P-Ch	— —	1.2 -1.2	V	T _J = 25°C, I _S = 1.3A, V _{GS} = 0V ③ T _J = 25°C, I _S = -1.3A, V _{GS} = 0V ③
t _{rr}	N-Ch P-Ch	— —	36 69	ns	N-Channel T _J = 25°C, I _F = 1.3A, di/dt = 100A/μs
Q _{rr}	N-Ch P-Ch	41 90	75 180	nC	P-Channel T _J = 25°C, I _F = -1.3A, di/dt = 100A/μs ③
t _{on}	N-P	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)			

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② N-Channel I_{SD} ≤ 3.5A, di/dt ≤ 90A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
P-Channel I_{SD} ≤ -2.3A, di/dt ≤ 90A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ Surface mounted on FR-4 board, t ≤ 10sec.

Dual N+ P Channel MOSFET

N-Channel

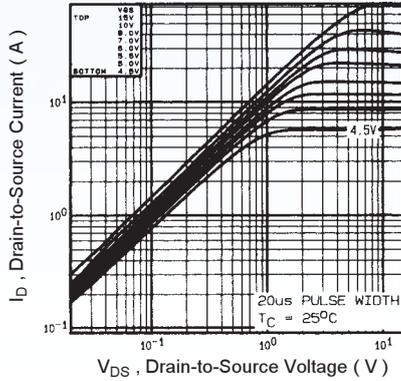


Fig 1. Typical Output Characteristics

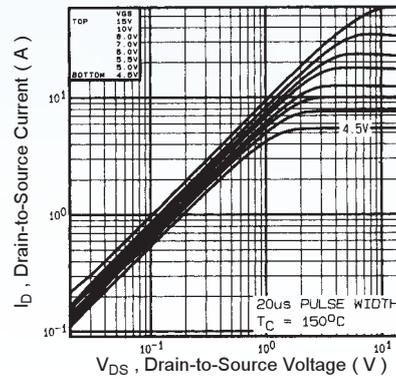


Fig 2. Typical Output Characteristics

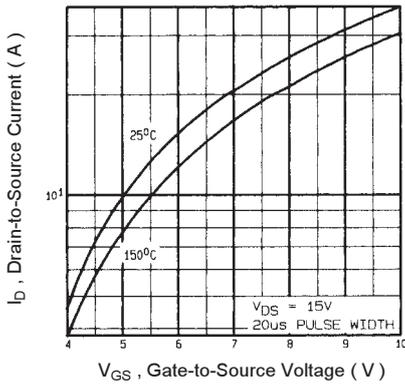


Fig 3. Typical Transfer Characteristics

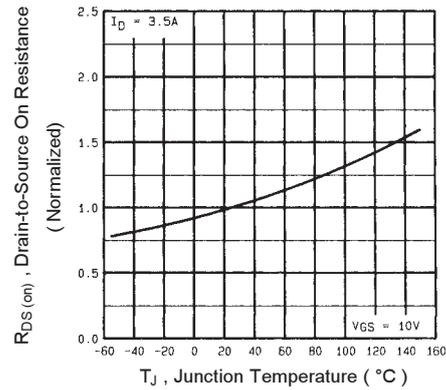


Fig 4. Normalized On-Resistance Vs. Temperature

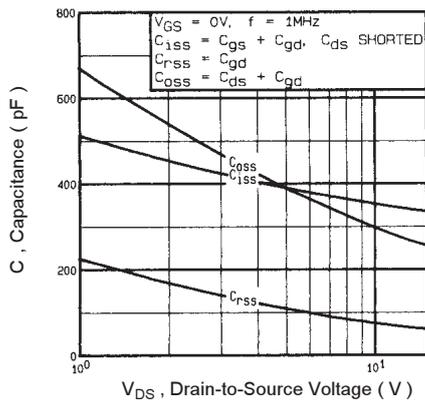


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

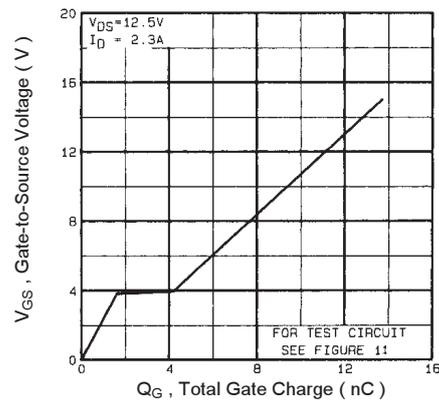


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

Dual N+ P Channel MOSFET

N-Channel

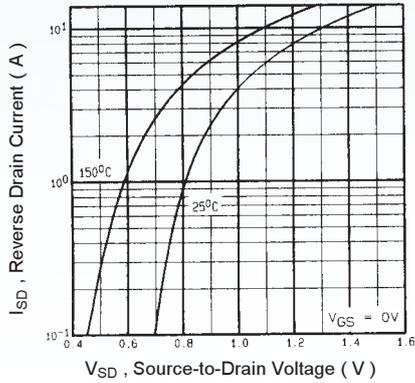


Fig 7. Typical Source-Drain Diode Forward Voltage

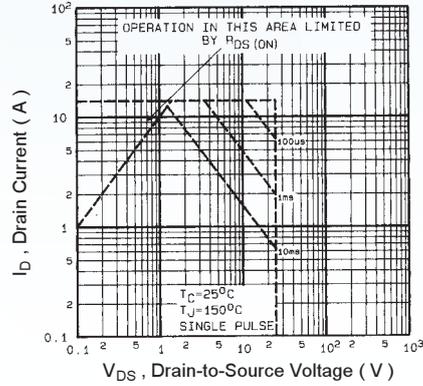


Fig 8. Maximum Safe Operating Area

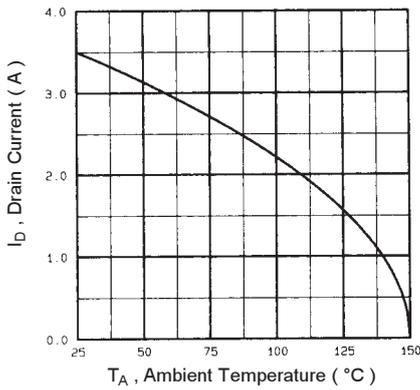


Fig 9. Maximum Drain Current Vs. Ambient Temperature

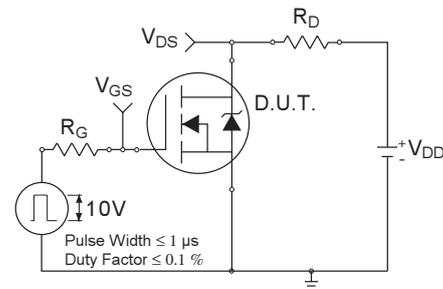


Fig 10a. Switching Time Test Circuit

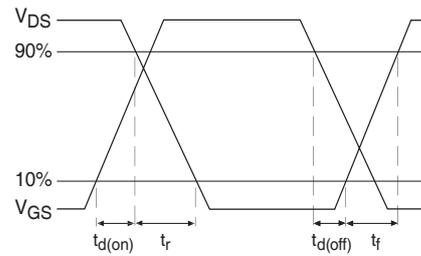


Fig 10b. Switching Time Waveforms

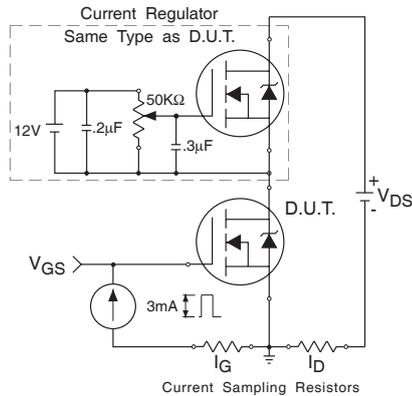


Fig 11a. Gate Charge Test Circuit

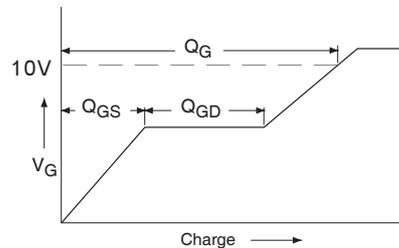


Fig 11b. Basic Gate Charge Waveform

Dual N+ P Channel MOSFET

P-Channel

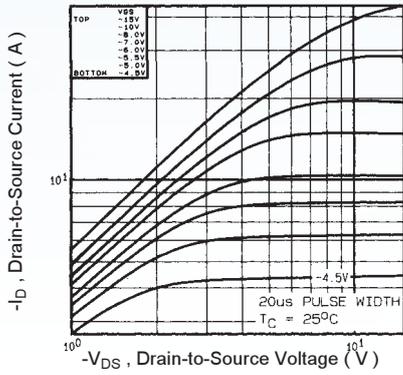


Fig 12. Typical Output Characteristics

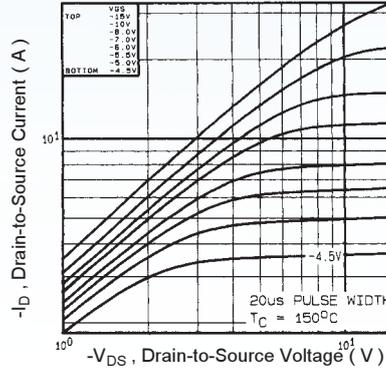


Fig 13. Typical Output Characteristics

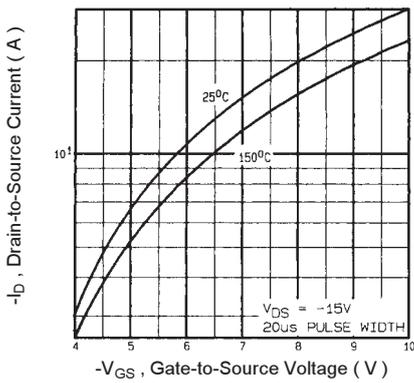


Fig 14. Typical Transfer Characteristics

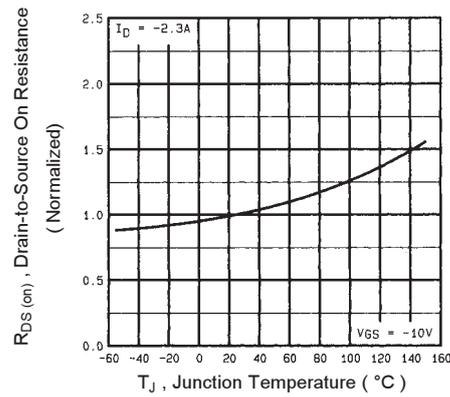


Fig 15. Normalized On-Resistance Vs. Temperature

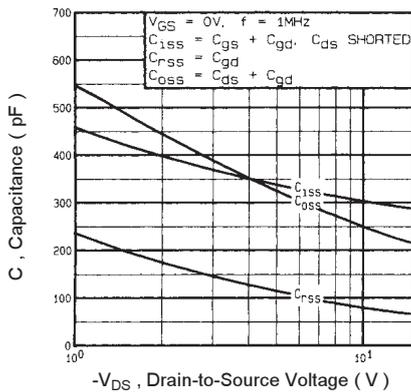


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

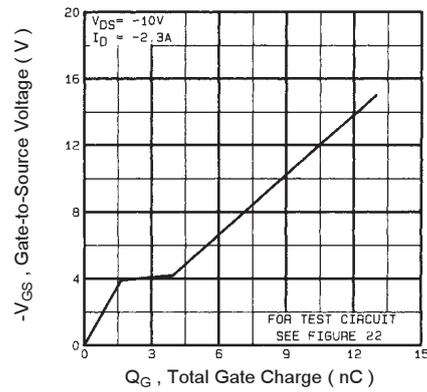


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

Dual N+ P Channel MOSFET

P-Channel

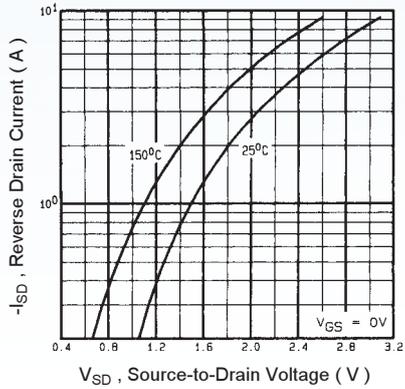


Fig 18. Typical Source-Drain Diode Forward Voltage

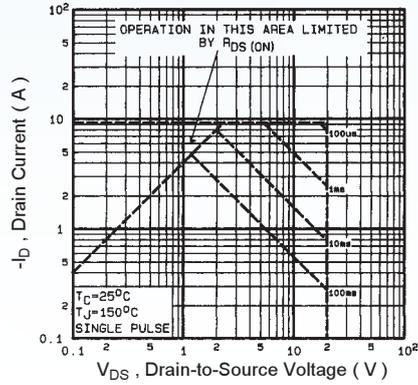


Fig 19. Maximum Safe Operating Area

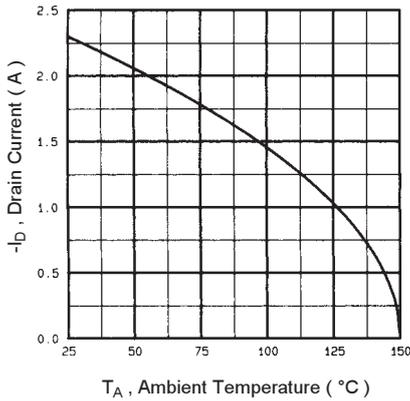


Fig 20. Maximum Drain Current Vs. Ambient Temperature

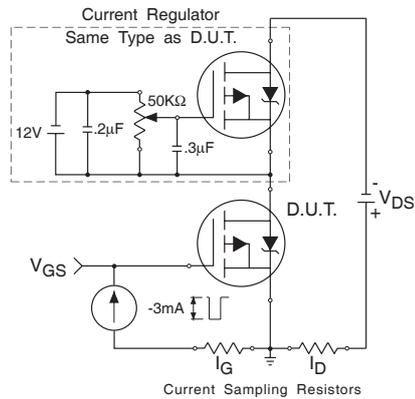


Fig 22a. Gate Charge Test Circuit

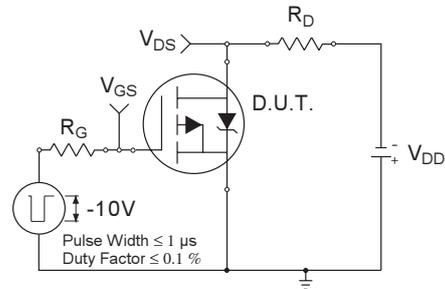


Fig 21a. Switching Time Test Circuit

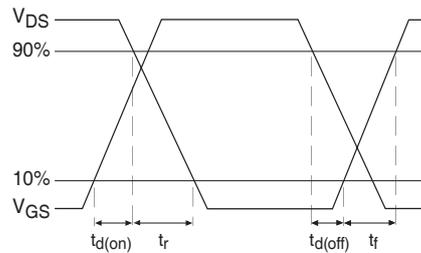


Fig 21b. Switching Time Waveforms

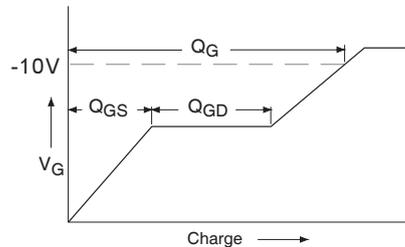


Fig 22b. Basic Gate Charge Waveform

Dual N + P Channel MOSFET

N & P-Channel

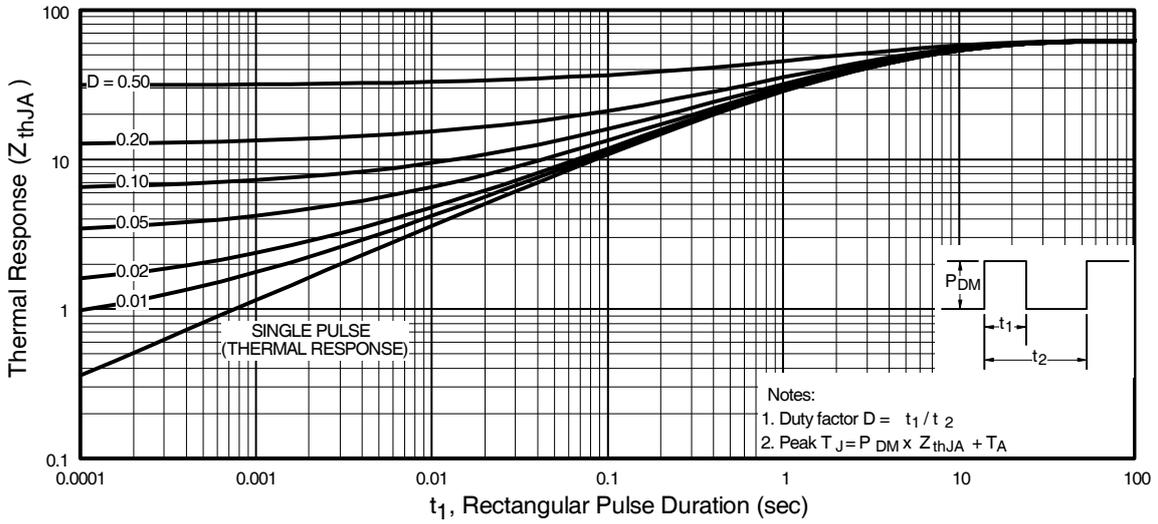
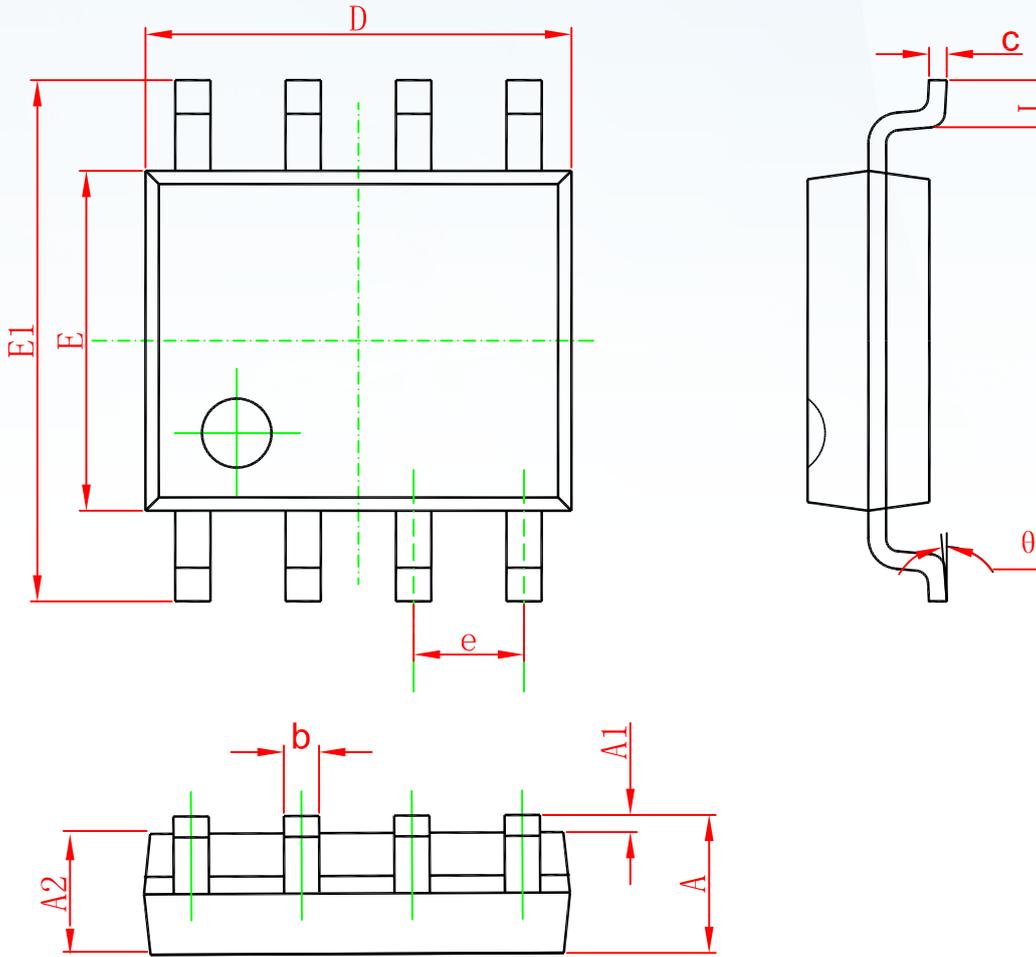


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

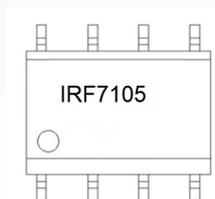
SOP-8

Dual N+ P Channel MOSFET



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Dual N+ P Channel MOSFET

Marking**Ordering information**

Order code	Package	Baseqty	Deliverymode
IRF7105	SOP-8	3000	Tape and reel

Disclaimer

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